# Lab 8 Design a MUX, and a High-Speed Full Adder

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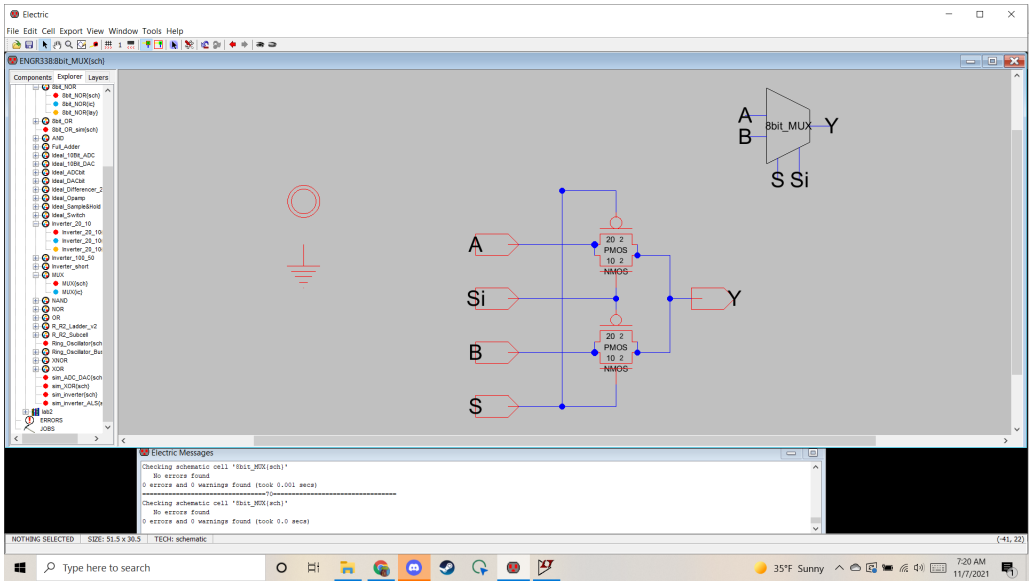
## 1 Introduction

Full Adders and MUX are an integral part of any circuit that requires basic arithmetic. In this lab, we will be going over the creation of a High Speed Full Adder.

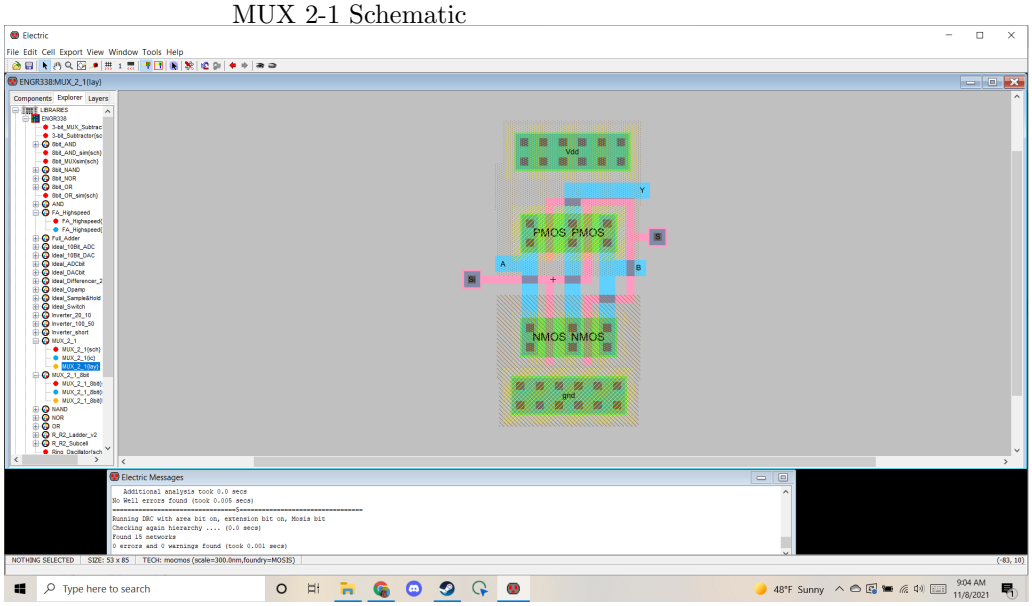
## 2 Materials and Methods

The tutorial for making these exact example in ElectricVLSI are found in /urlhttp://www.yilectronics.com/Courses/ENGR338L$_C E/f$2021/$lab8_M UX_F AII/Lab8.html$

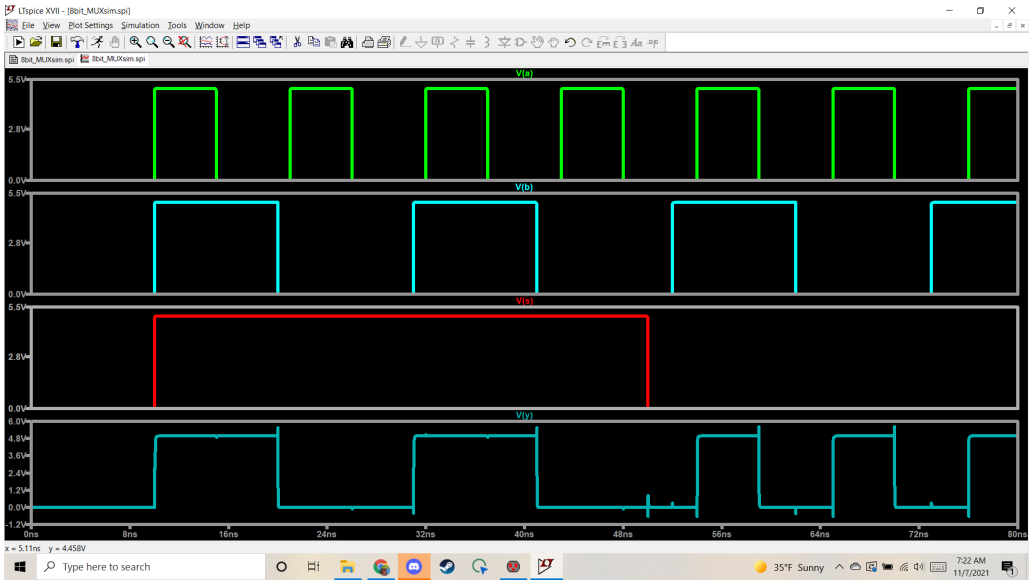
# 3 Results



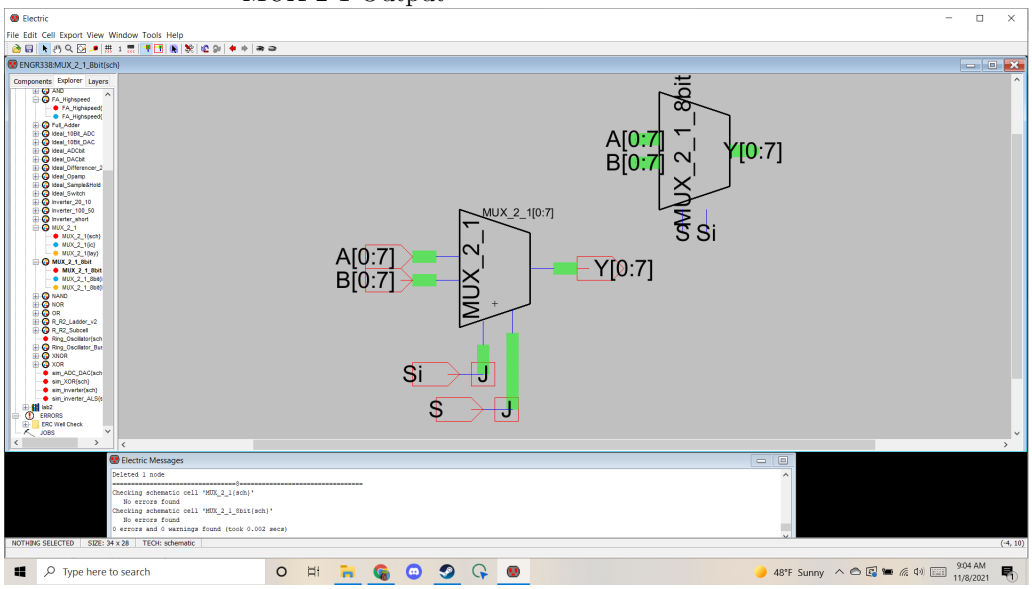

MUX 2-1 Schematic



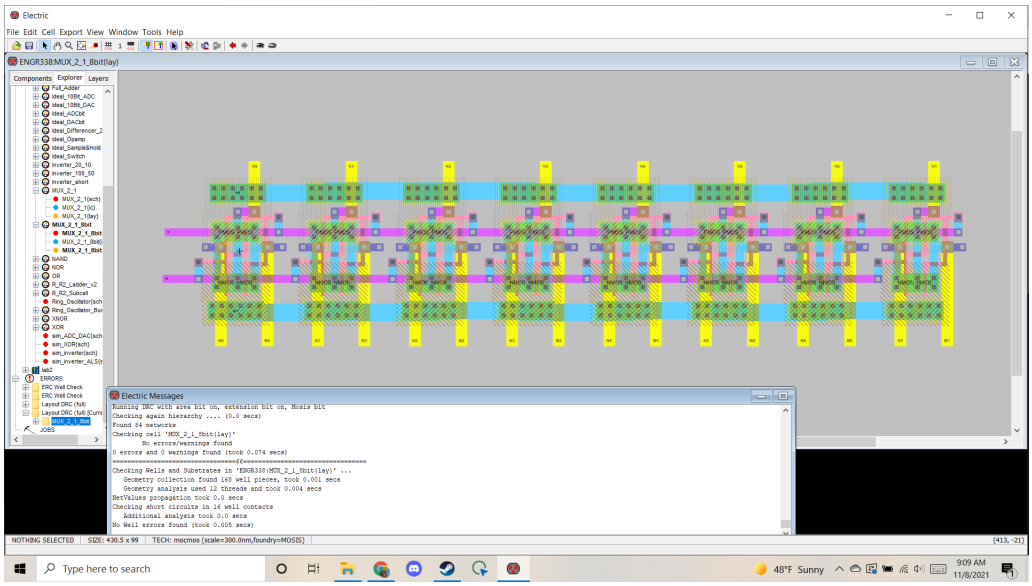

MUX 2-1 Layout



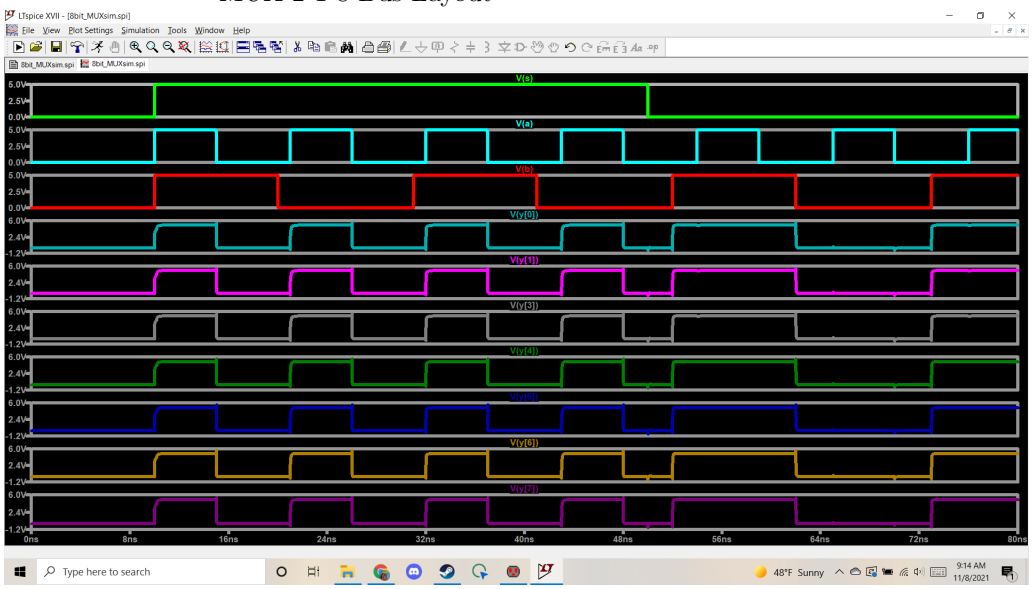

MUX 2-1 Output



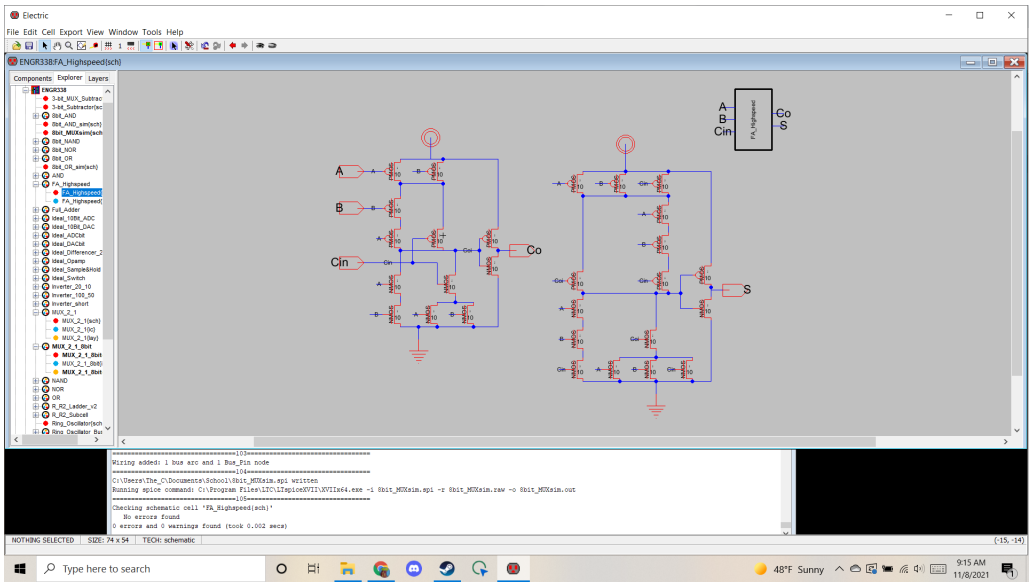

MUX 2-1 8 Bus



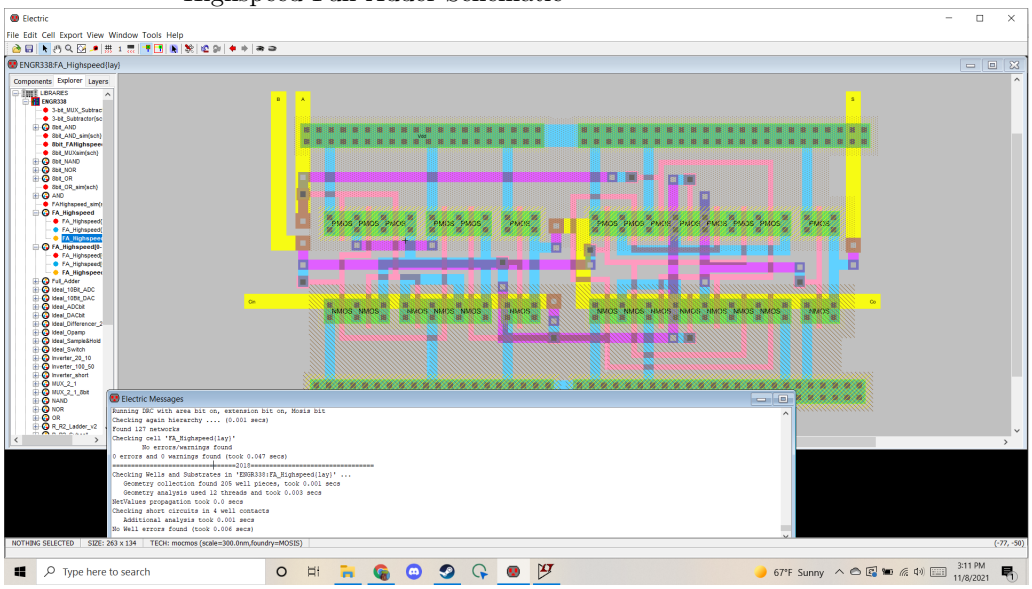

MUX 2-1 8 Bus Layout



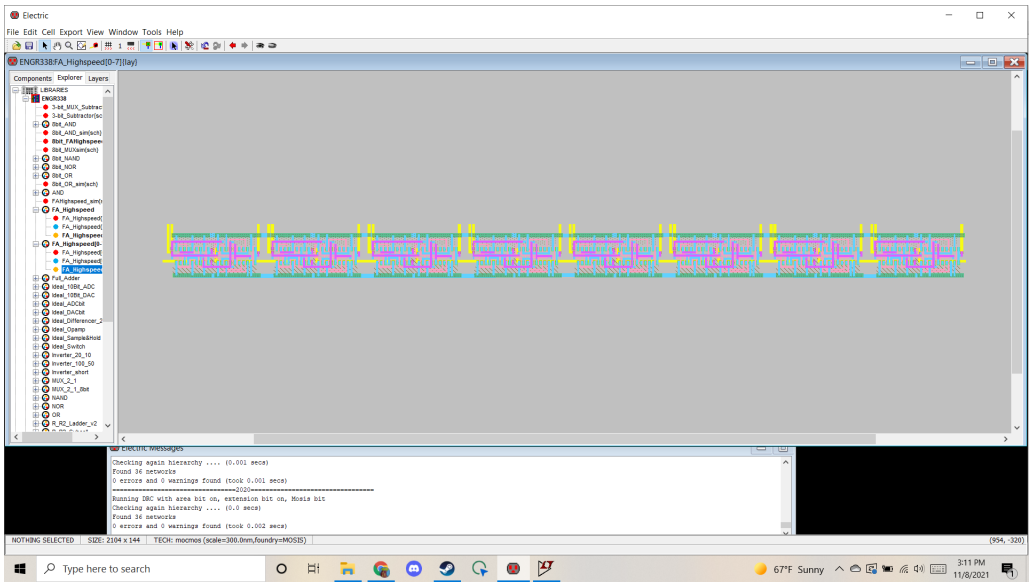

MUX 2-1 8 Bus Output



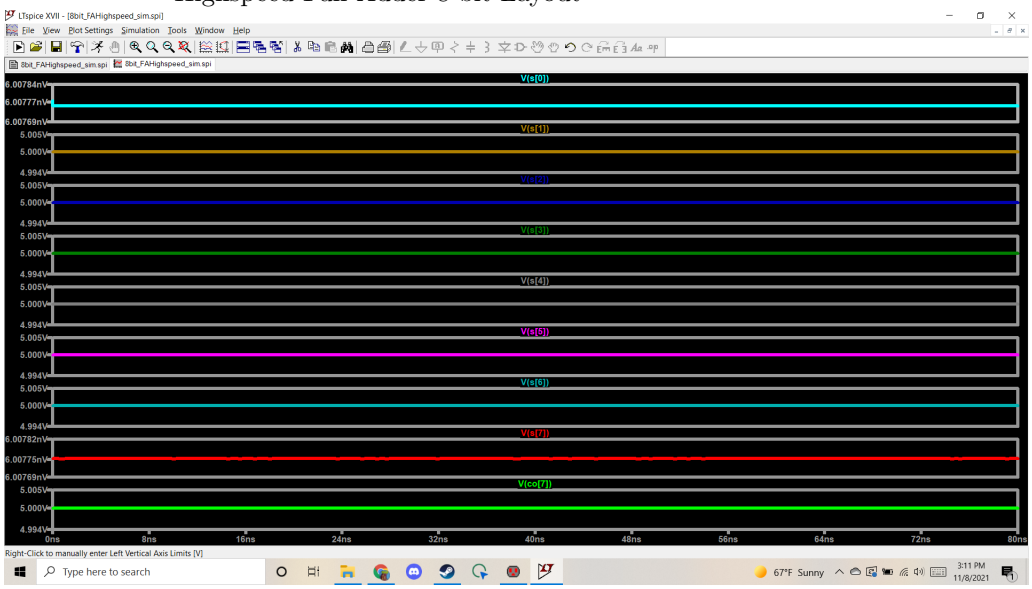

Highspeed Full Adder Schematic




Highspeed Full Adder Layout



Highspeed Full Adder 8-bit Layout



Highspeed Full Adder 8-bit Output

# 4 Discussion

As you can see, all the the outputs are correct and all the checks come clean, so these schematics and layouts work. I'm not sure if you actually read these, but I don't know where the NCC hierarchical checks is, so thats why they're

not there.