

Lab 9 Design a Simple 8-Bit ALU

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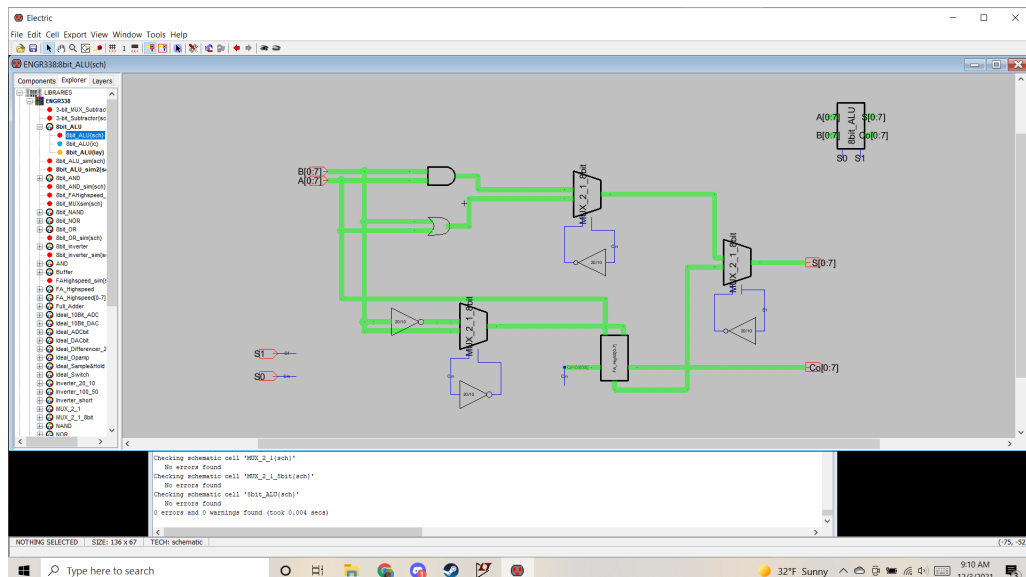
1 Introduction

ALU stands for Arithmetic Logic Unit. This device is designed to add and subtract parallel bit sequences. ALUs are required for most circuits and in of themselves, basic calculators.

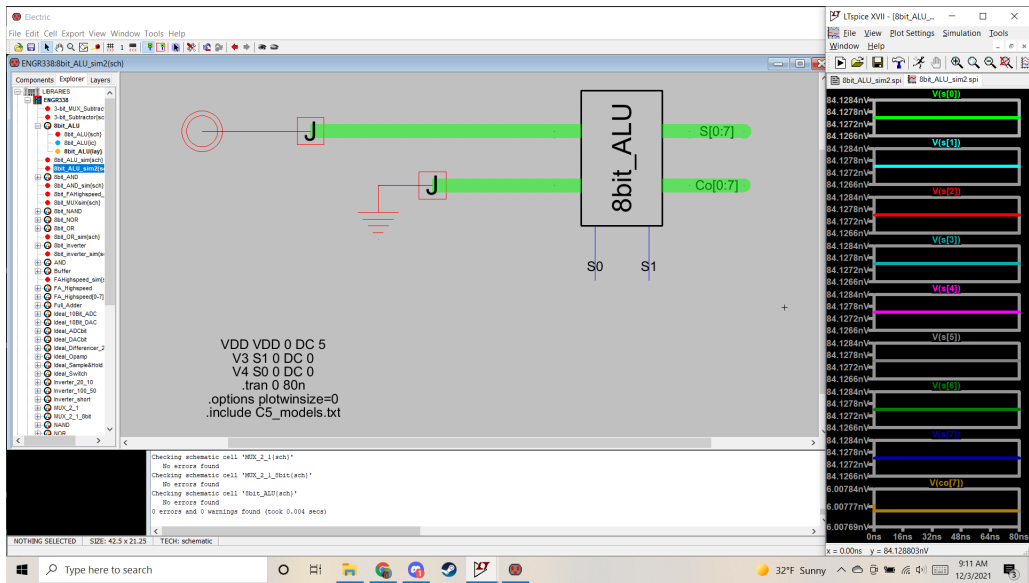
2 Materials and Methods

The tutorial for making this example in ElectricVLSI are found in <http://www.yilelectronics.com/Courses/EN>

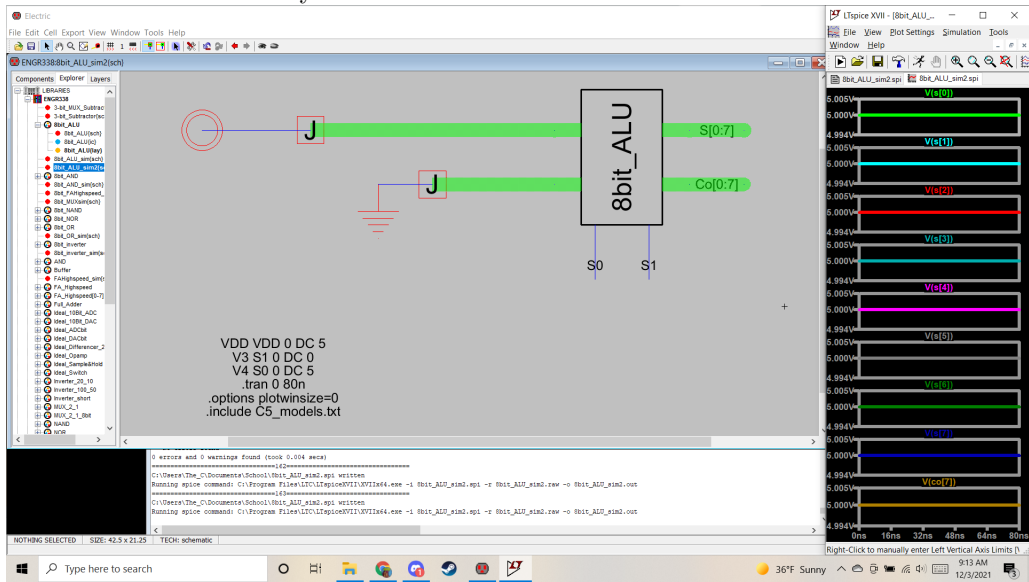
3 Results



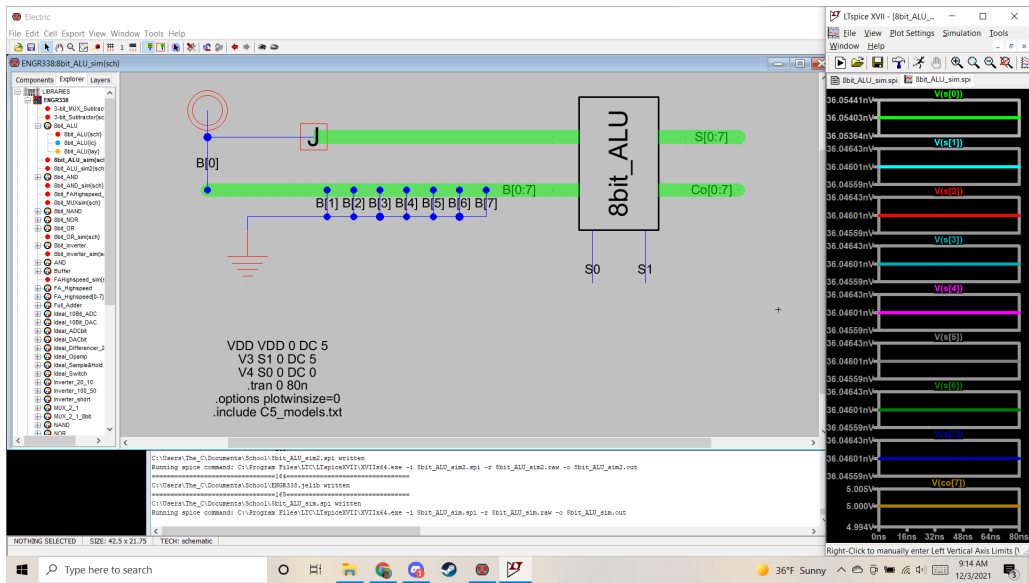
ALU Schematic



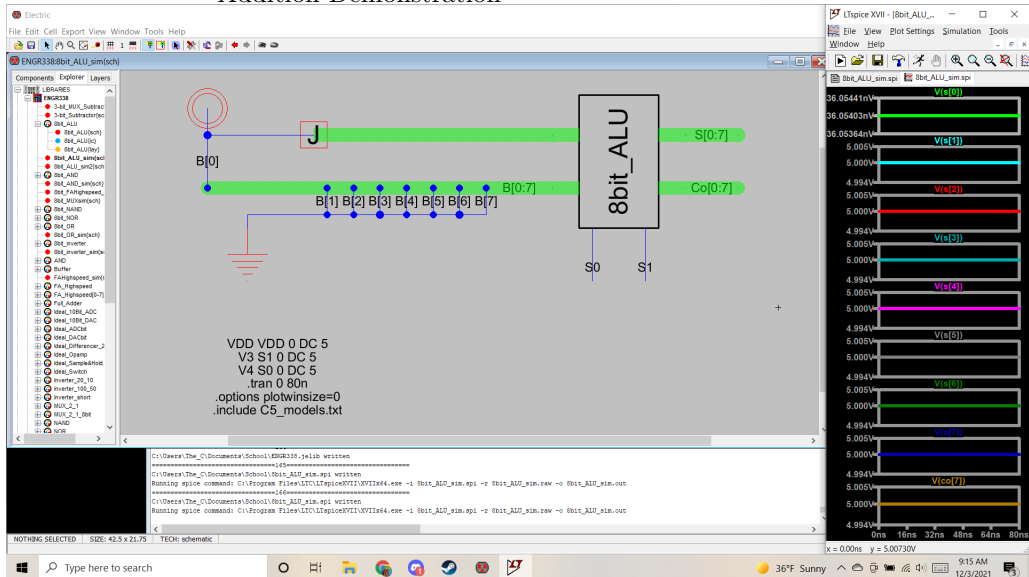
Verify AND Gate



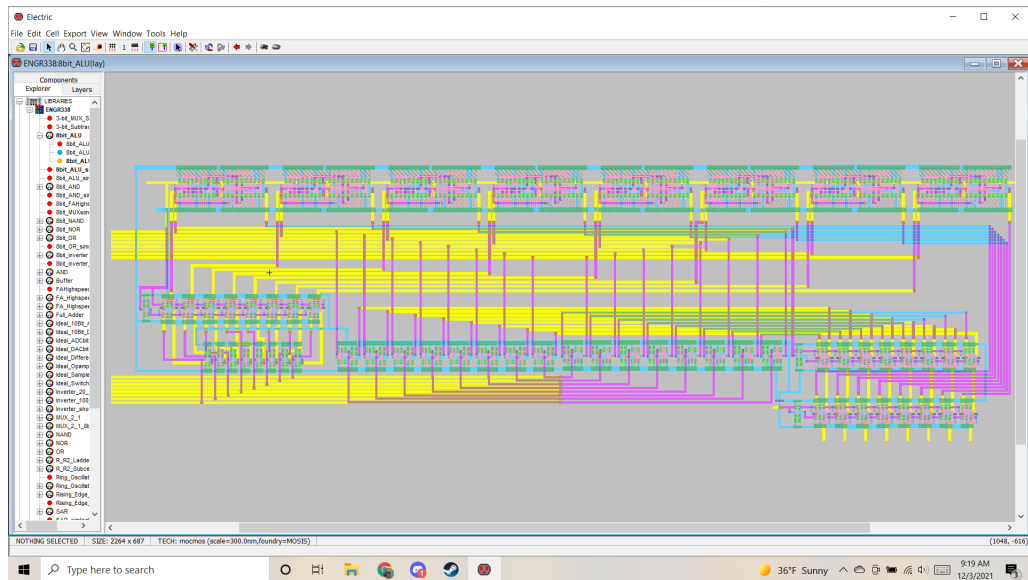
Verify OR Gate



Addition Demonstration



Subtraction Demonstration



ALU Layout

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Electric Messages
=====208=====
Running DRC with area bit on, extension bit on, Hosis bit
Checking again hierarchy .... (0.0 secs)
Found 88 networks
Checking cell '8bit_ALU[lay]'
No errors/warnings found
0 errors and 0 warnings found (took 0.285 secs)
=====209=====
Running DRC with area bit on, extension bit on, Hosis bit
Checking again hierarchy .... (0.0 secs)
Found 88 networks
0 errors and 0 warnings found (took 0.002 secs)
=====210=====
Checking Wells and Substrates in 'ENGR338:8bit_ALU[lay]' ...
Geometry collection found 2704 well pieces, took 0.005 secs
Geometry analysis used 12 threads and took 0.009 secs
NetValues propagation took 0.001 secs
Checking short circuits in 118 well contacts
Additional analysis took 0.0 secs
FOUND 16 WELL ERRORS (took 0.016 secs)
ERC Well Check found 16 errors, 0 warnings!
Type > and < to step through errors, or open the ERRORS view in the explorer
=====211=====
Hierarchical NCC every cell in the design: cell '8bit_ALU[sch]' cell '8bit_ALU[lay]'
Comparing: ENGR338:AND[sch] with: ENGR338:AND[lay]
exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338:8bit_AND[sch] with: ENGR338:8bit_AND[lay]
exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338:OR[sch] with: ENGR338:OR[lay]
exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338:8bit_OR[sch] with: ENGR338:8bit_OR[lay]
exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338:Inverter_short[sch] with: ENGR338:Inverter_short[lay]
exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338:8bit_inverter[sch] with: ENGR338:8bit_inverter[lay]
exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338:FA_Highspeed[sch] with: ENGR338:FA_Highspeed[lay]
exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: ENGR338:FA_Highspeed[0-7][sch] with: ENGR338:FA_Highspeed[0-7][lay]
exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338:Inverter_20_10[sch] with: ENGR338:Inverter_20_10[lay]
exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338:MUX_2_1_8bit[sch] with: ENGR338:MUX_2_1_8bit[lay]
exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: ENGR338:8bit_ALU[sch] with: ENGR338:8bit_ALU[lay]
exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.014 seconds.

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Error Check

4 Discussion

The functionality of the ALU works great, however the DRC has 16 errors because the inverters with the AND and OR gates have 1 error. This error is "No P-Well contact in this area" on the NMOS side. I have tried everything to try and resolve this error, but no matter how much more pure P-Well-Nodes I add or how many times I rebuild it, I get the same error. Other than that one error, everything else worked great and the error messages that were not included in the previous labs were resolved here