Build a NAND, NOR, XOR, and Full Adder

Calvin Reese
cjreese@fortlewis.edu

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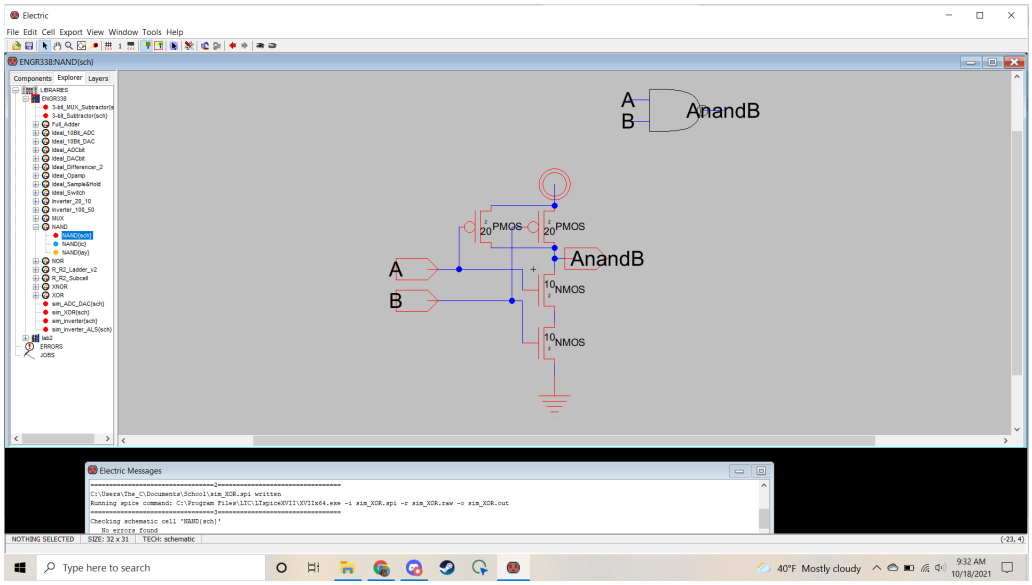
1 Introduction

In this lab, we will be creating layouts of the NAND, NOR, and XNOR gates to make a layout of a full adder then testing their output.

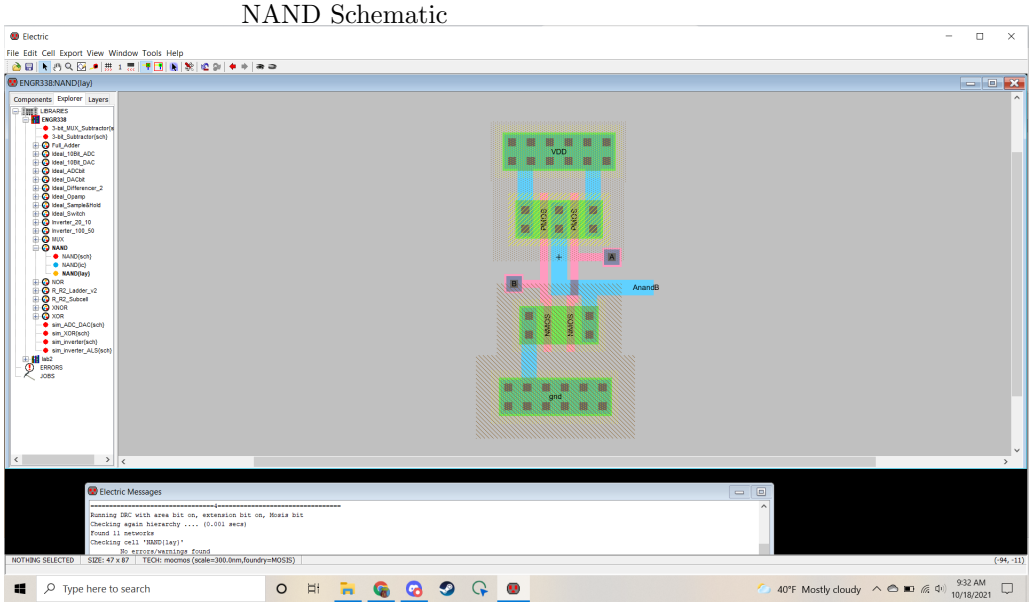
2 Materials and Methods

The instructions to create these layouts are on the webpage `http://www.yilectronics.com/Courses/ENGR338L_CE/f2021/lab6_NAND_NOR_XOR_FA/Lab6.html` **Electric VLSI is used to design the output and LTSpice is used to model the output.**

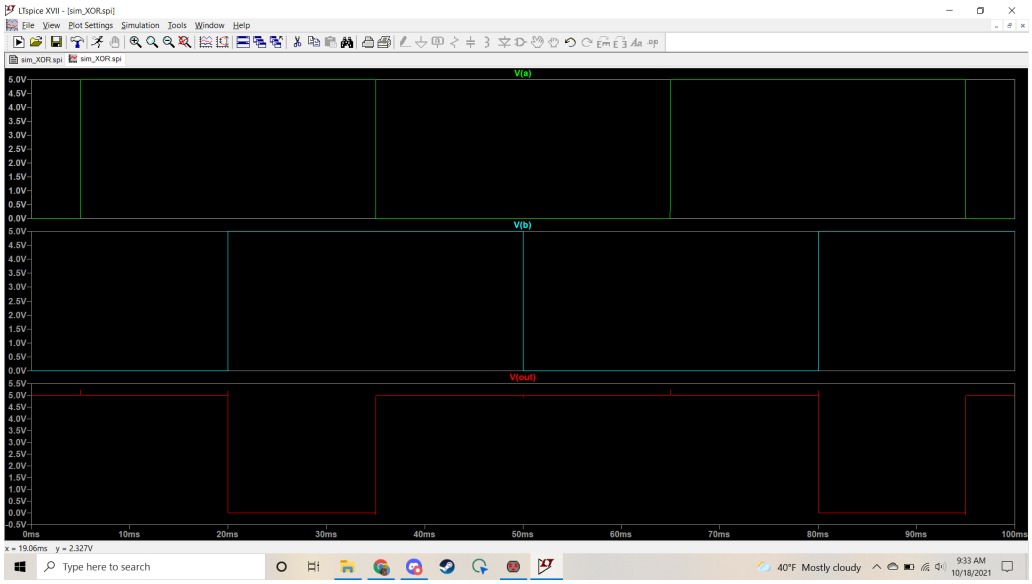
3 Results



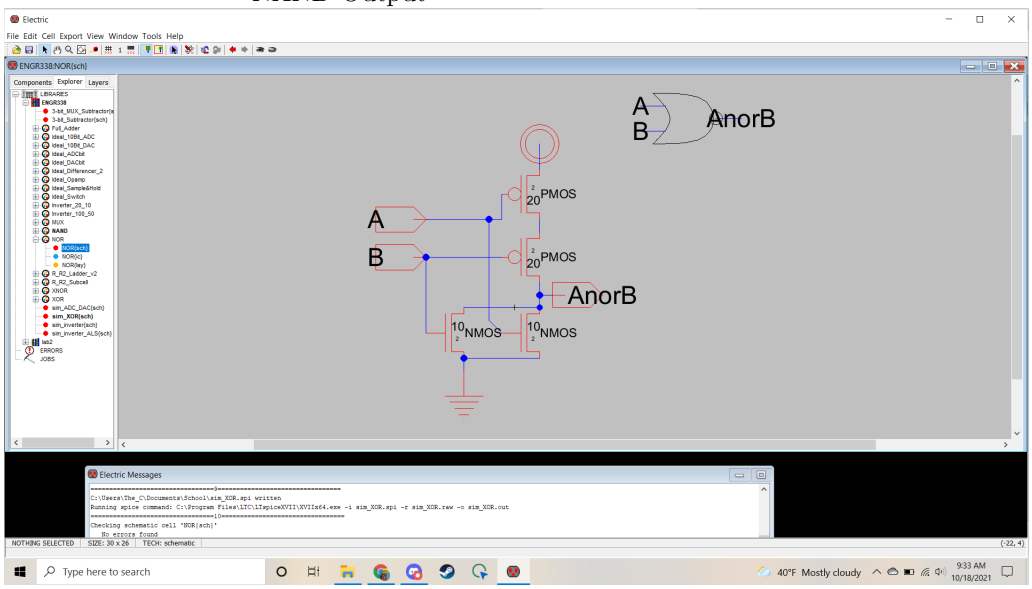
NAND Schematic



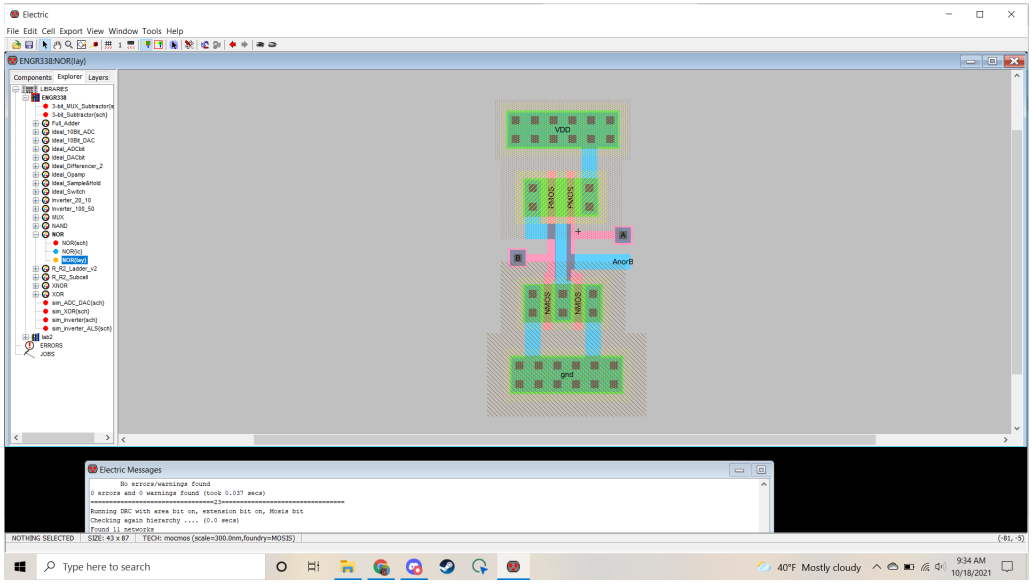
NAND Layout



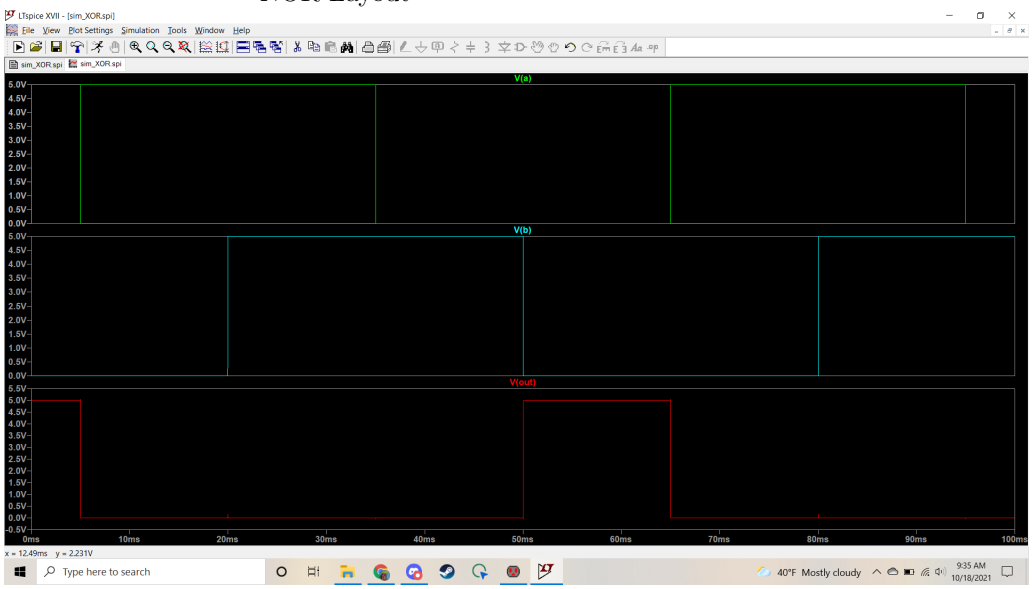
NAND Output



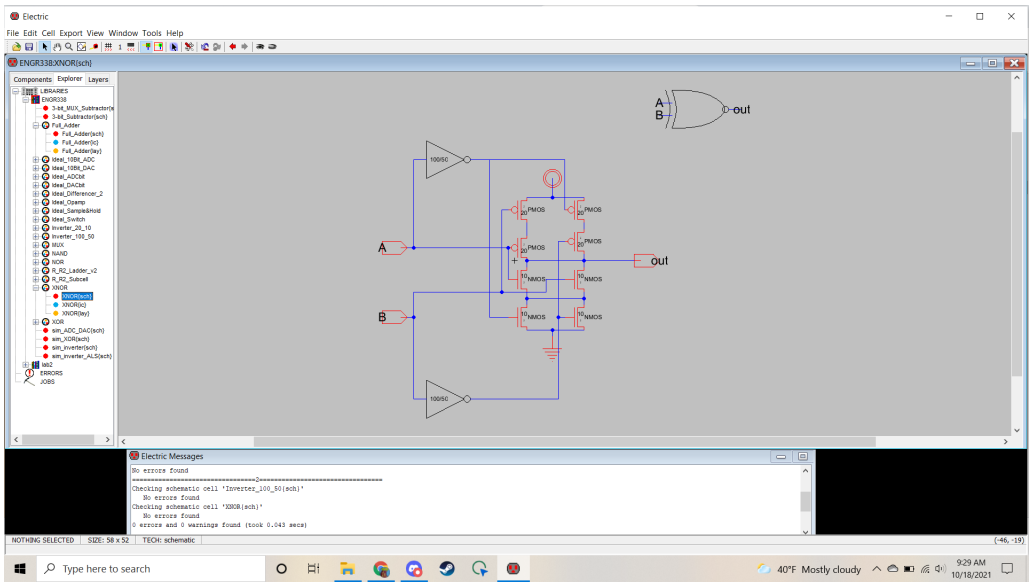
NOR Schematic



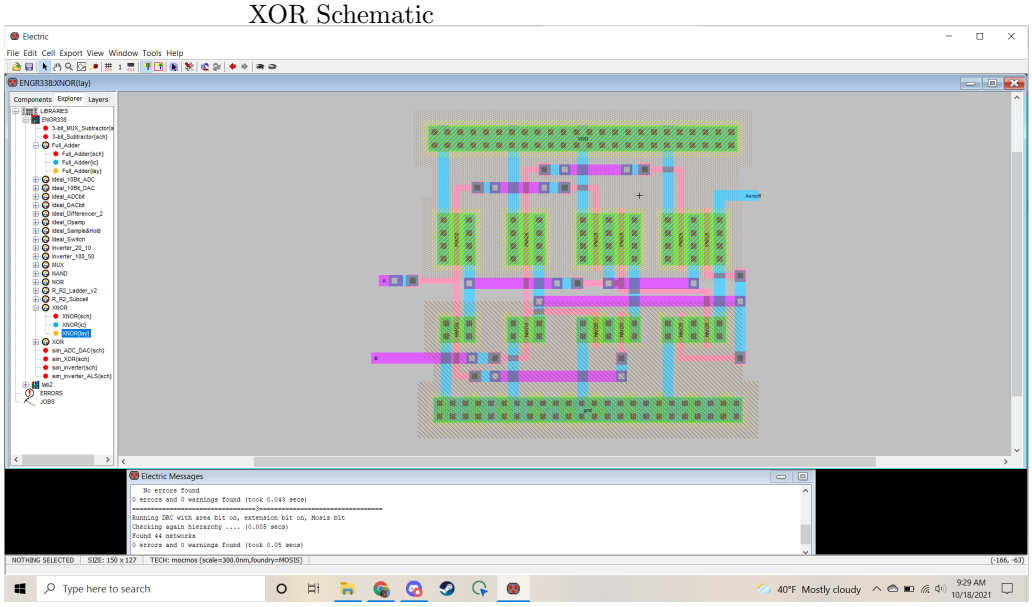
NOR Layout



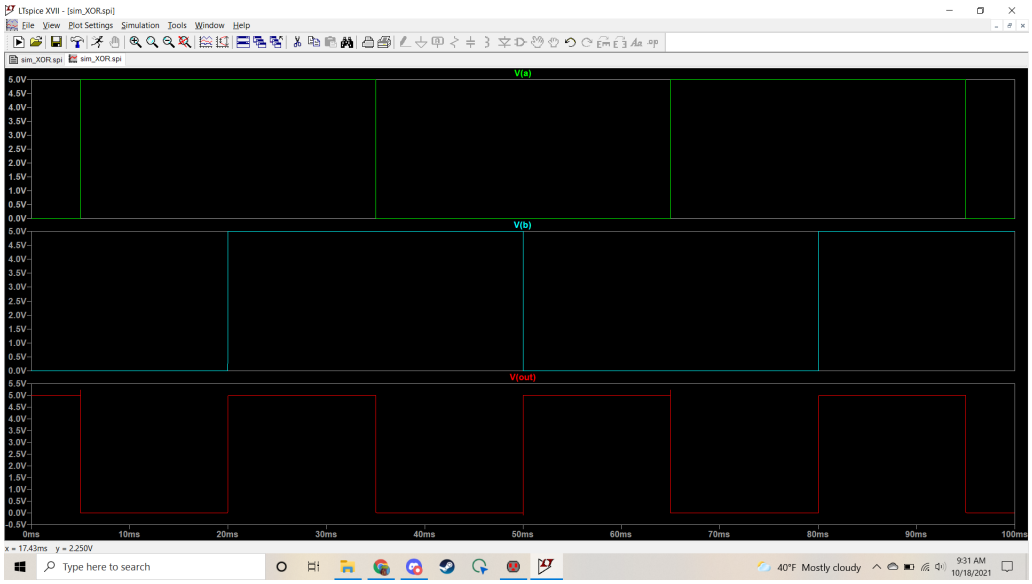
NOR Output



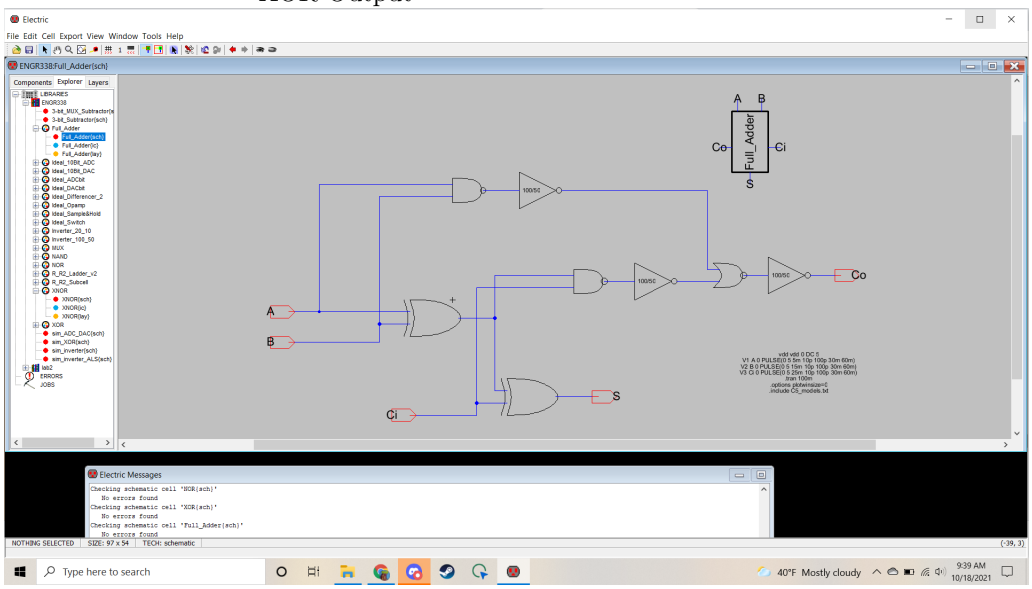
XOR Schematic



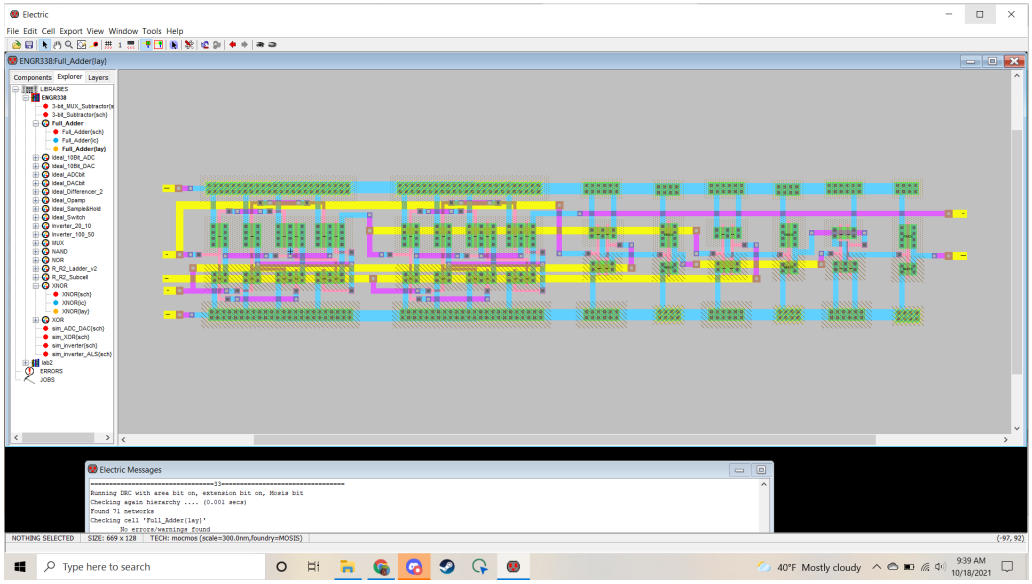
XOR Layout



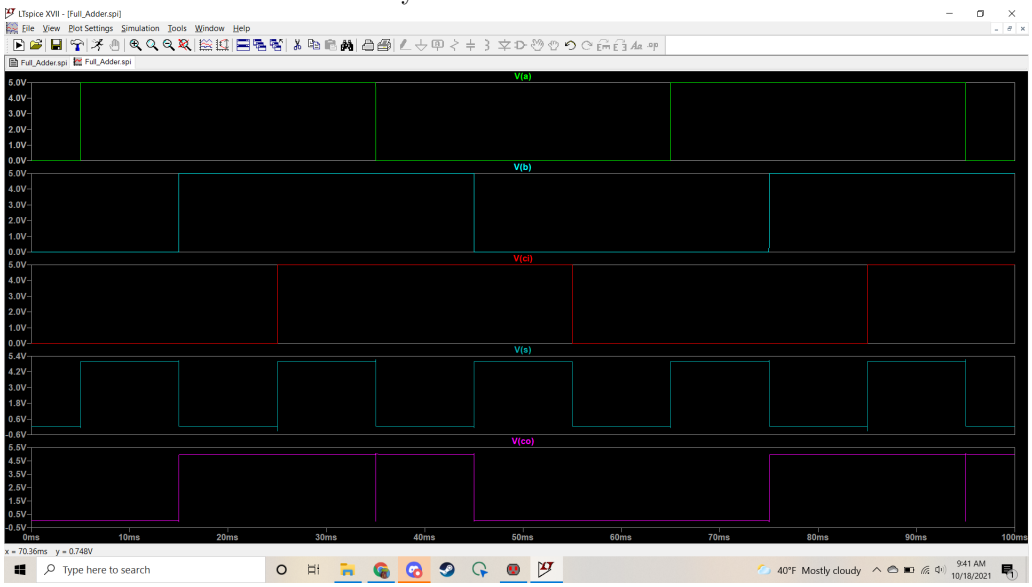
XOR Output



Full Adder Schematic



Full Adder Layout



Full Adder Output

4 Discussion

As seen above, the output of each component follows the correct logic, therefore all the schematics and layouts were successful.