The Inverter

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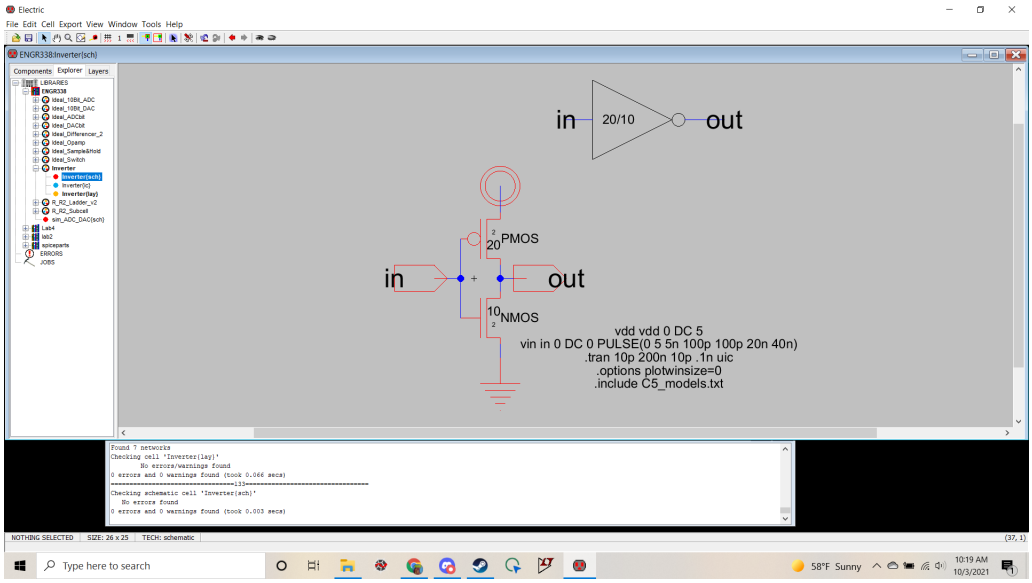
1 Introduction

MOSFETS are used everywhere and the more effective and simple form of MOSFETS are CMOS Inverters. These inverters use one PMOS to pass logic high and one NMOS to pass logic low. In this lab we will be going over the process of drawing an inverter in Electric VLSI and simulating it in both LTSpice and Electric VLSI.

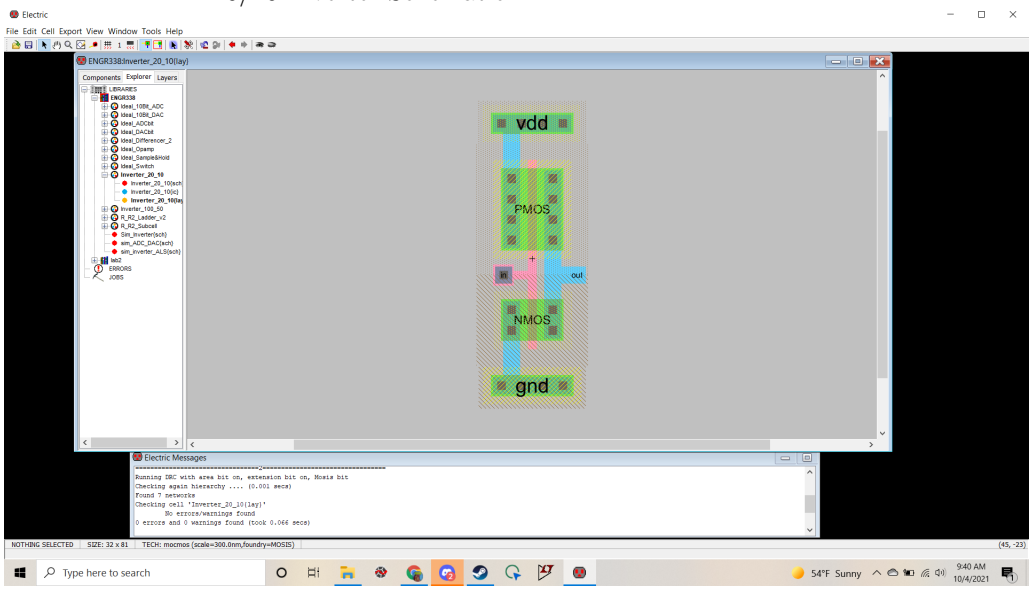
2 Materials and Methods

We went through 5 tasks as per the instructions in `http://www.yilectronics.com/Courses/ENGR338L_CE/f2021/lab5_Inverter/Lab5.html`. These tasks go over creating 2 different inverters (one larger and one smaller) then testing both of them in LTSpice and Electric VLSM.

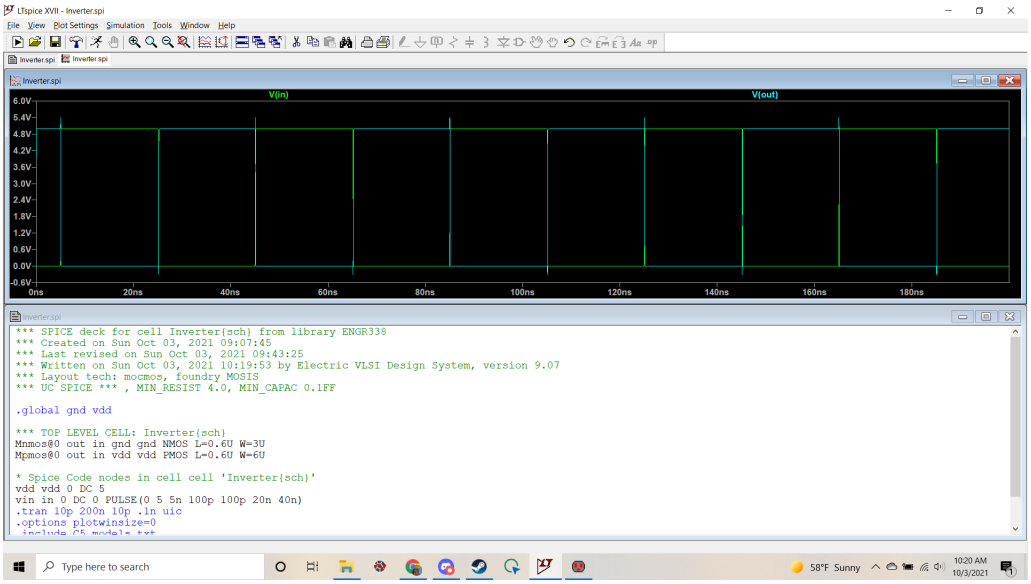
3 Results



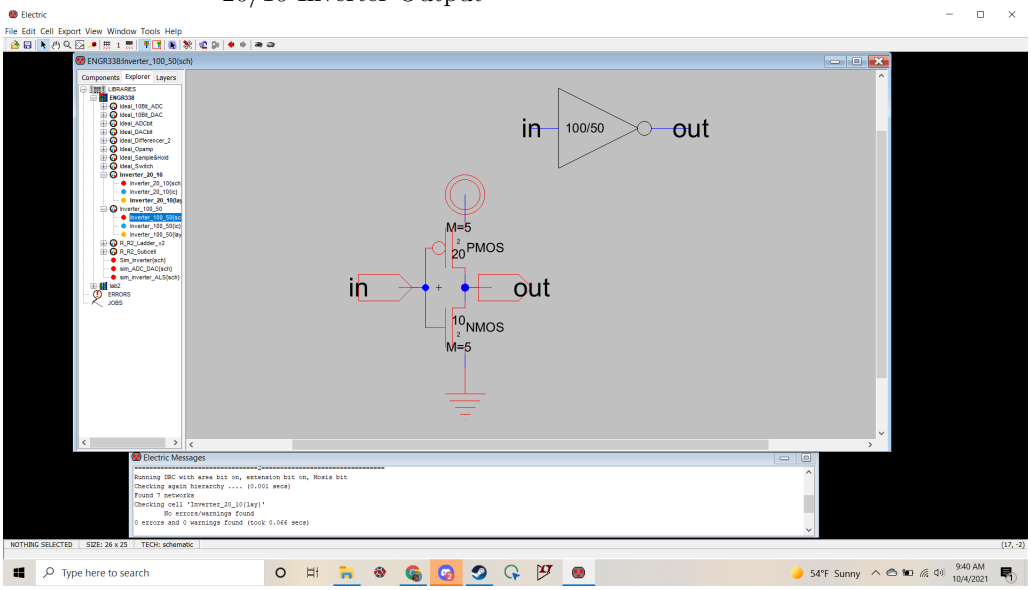
20/10 Inverter Schematic



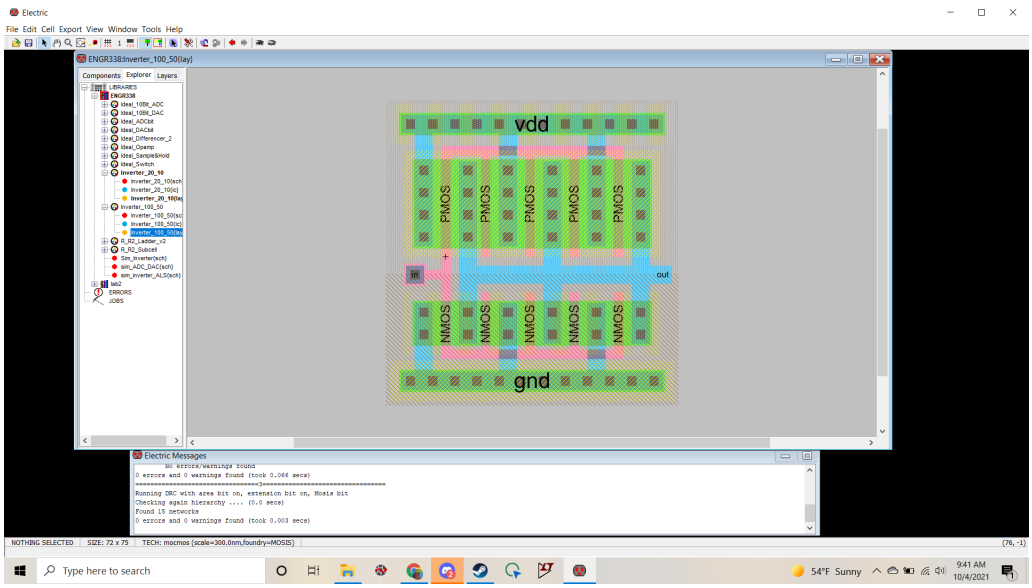
20/10 Inverter Layout



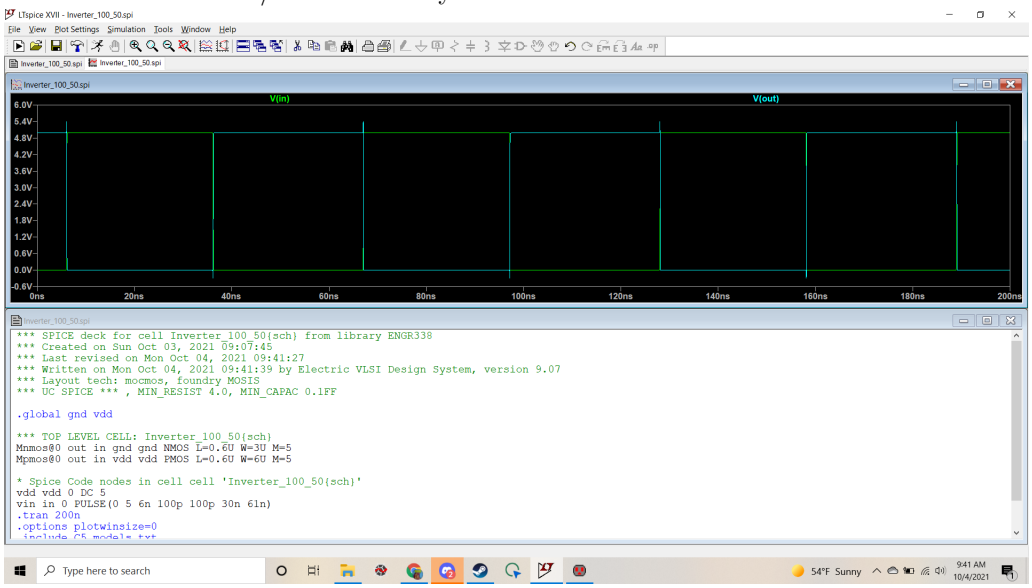
20/10 Inverter Output



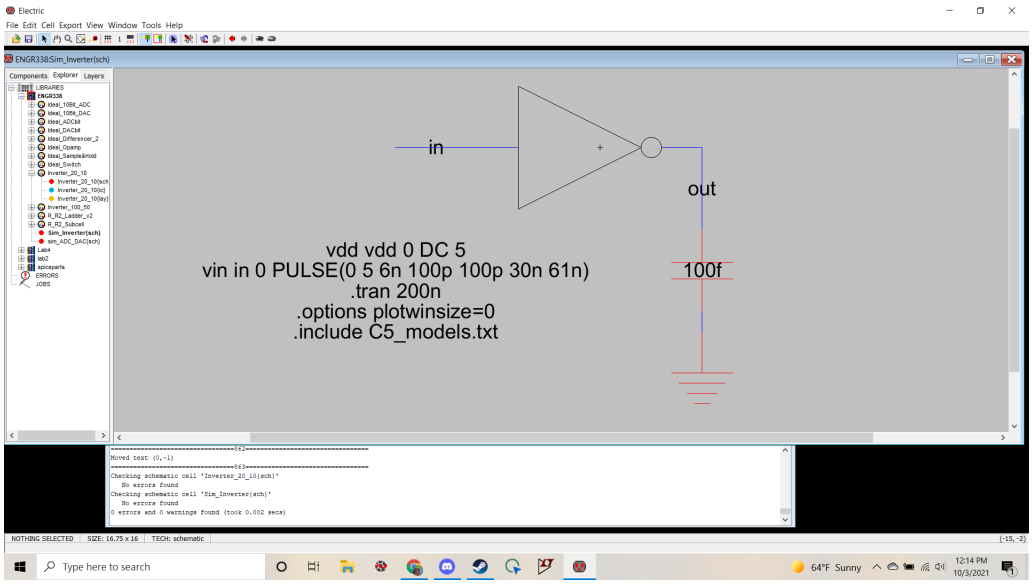
100/50 Inverter Schematic



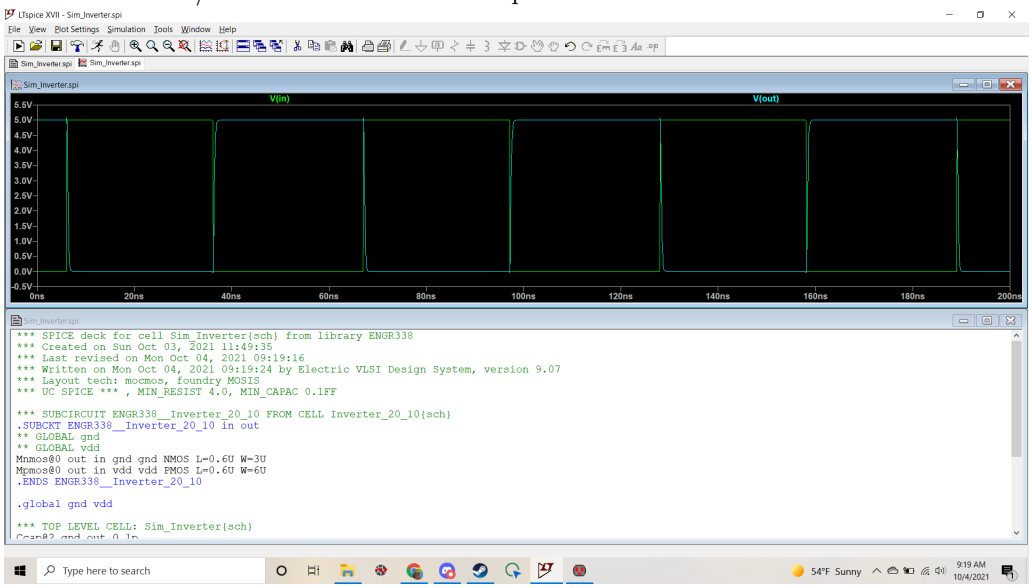
100/50 Inverter Layout



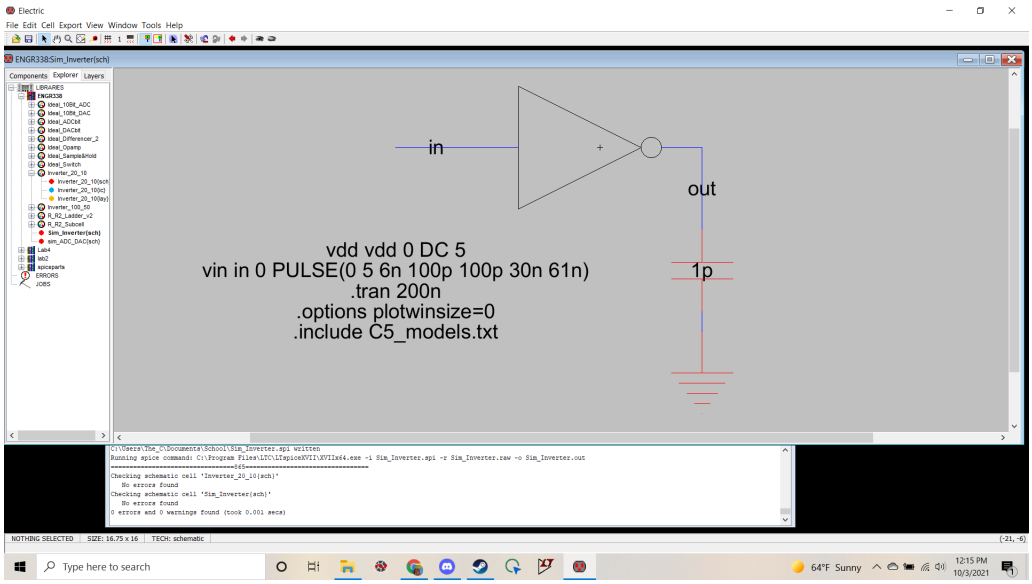
100/50 Inverter output



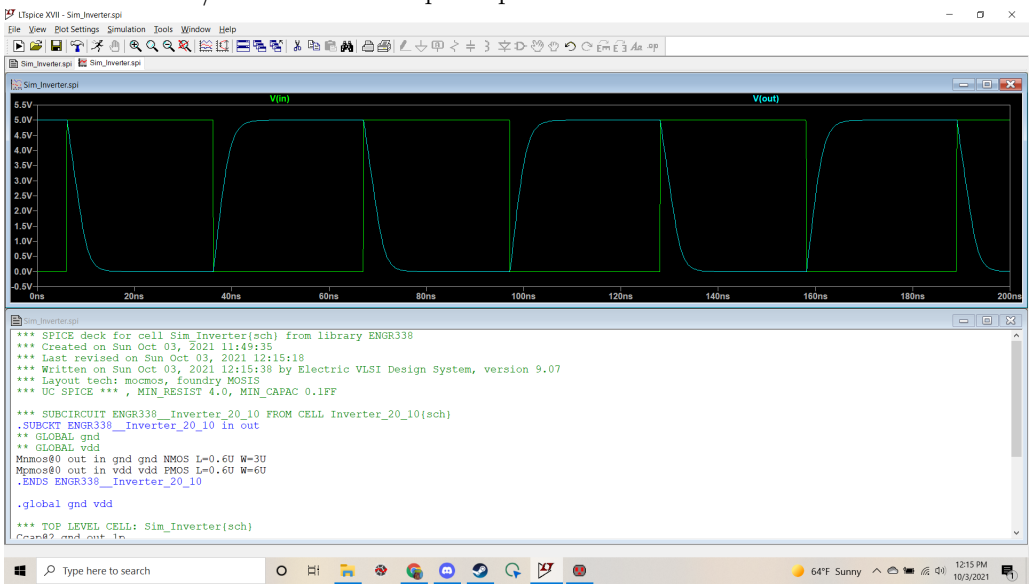
20/10 Inverter with 100fF Capacitor



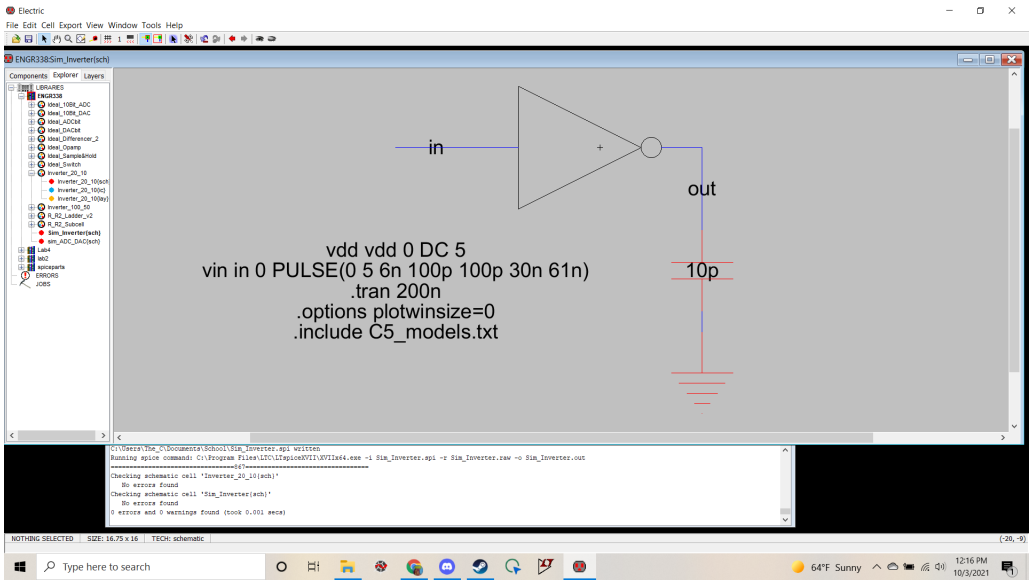
20/10 Inverter with 100fF Capacitor Output



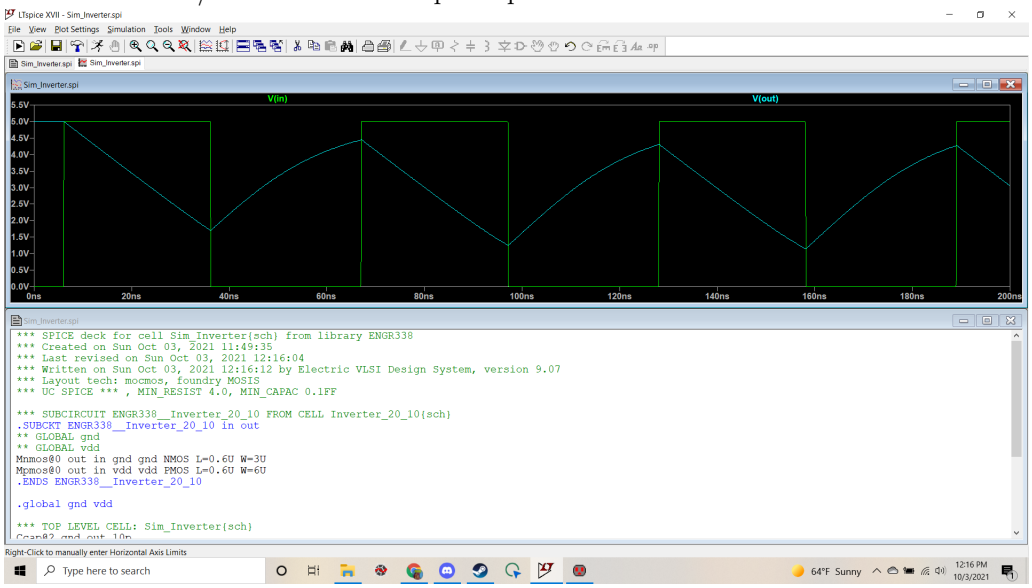
20/10 Inverter with 1pF Capacitor



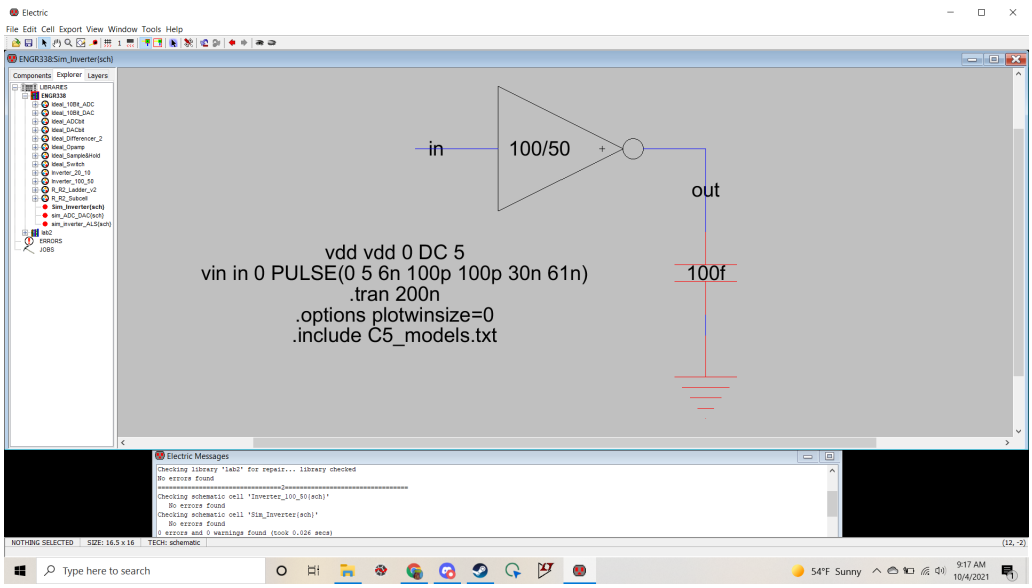
20/10 Inverter with 1pF Capacitor Output



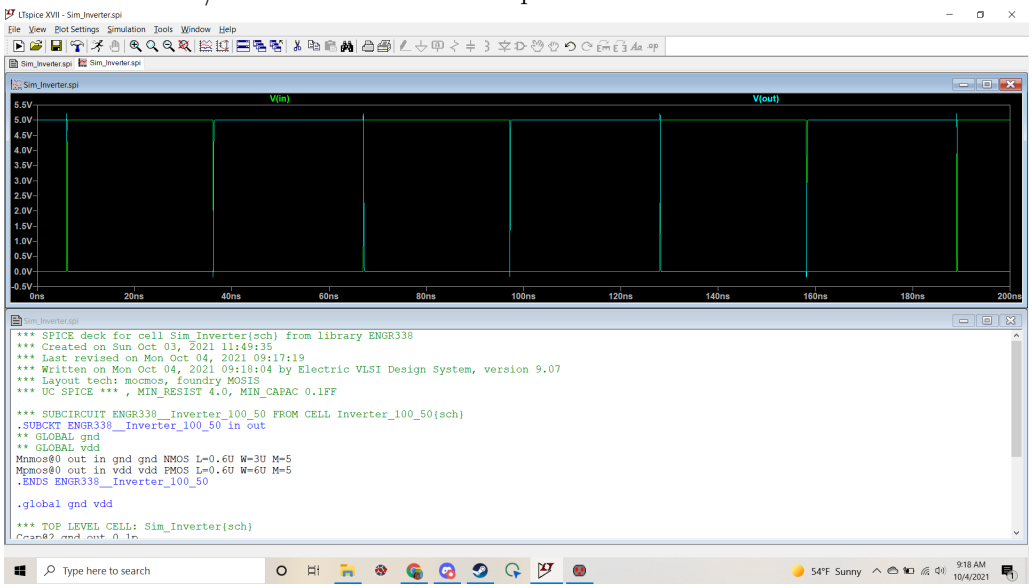
20/10 Inverter with 10pF Capacitor



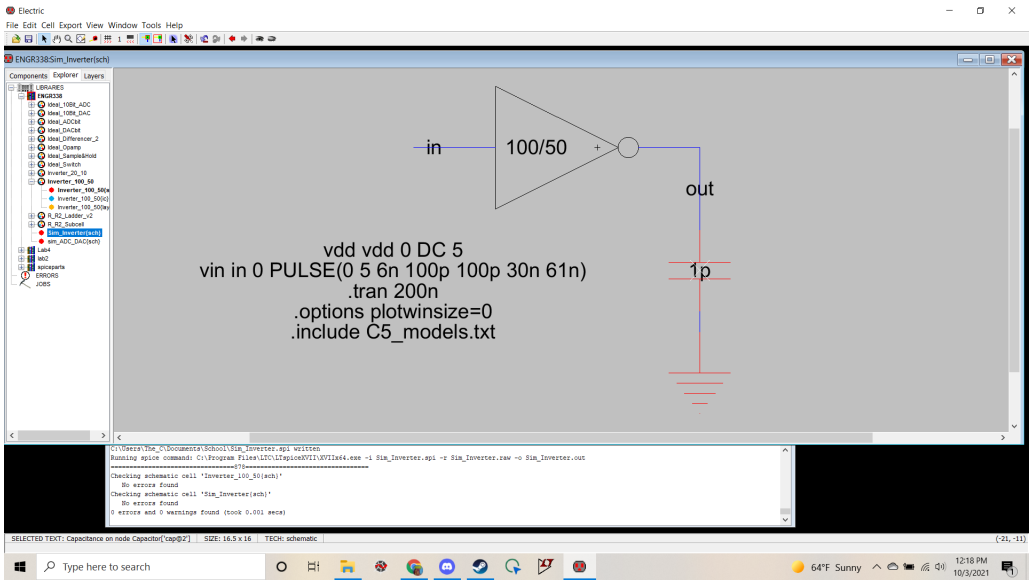
20/10 Inverter with 10pF Capacitor Output



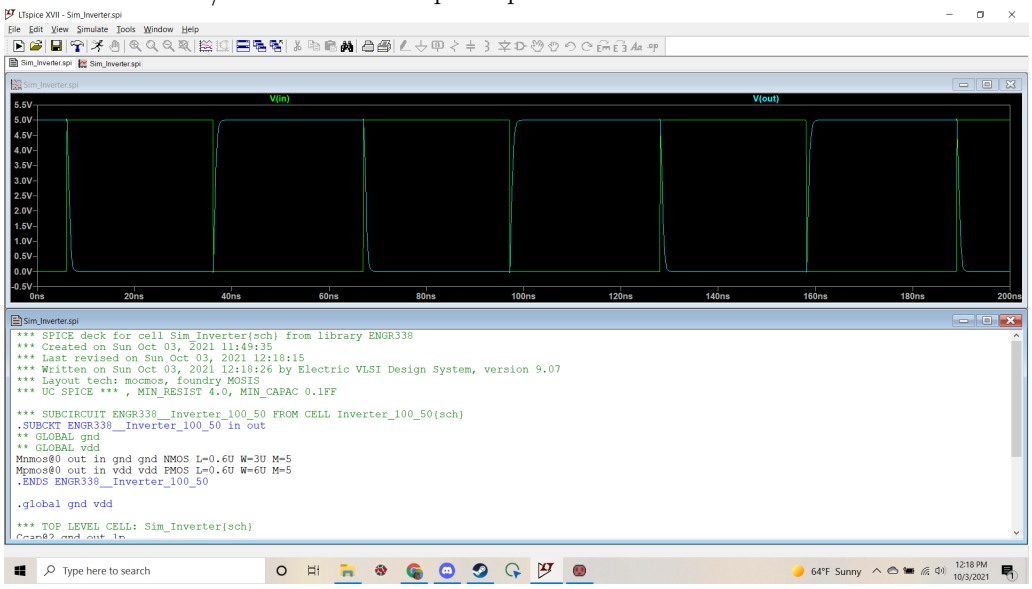
100/50 Inverter with 100fF Capacitor



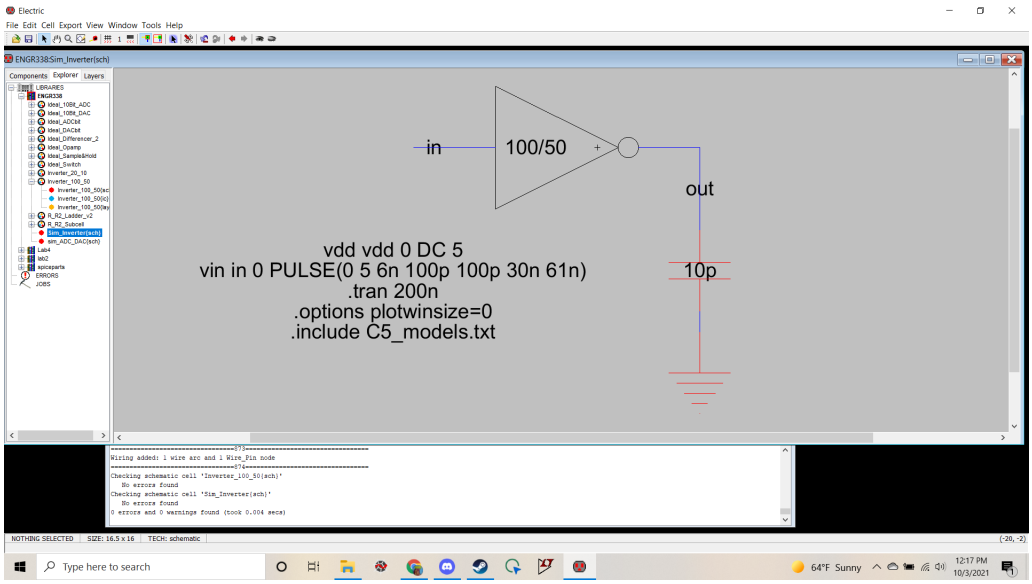
100/50 Inverter with 100fF Capacitor Output



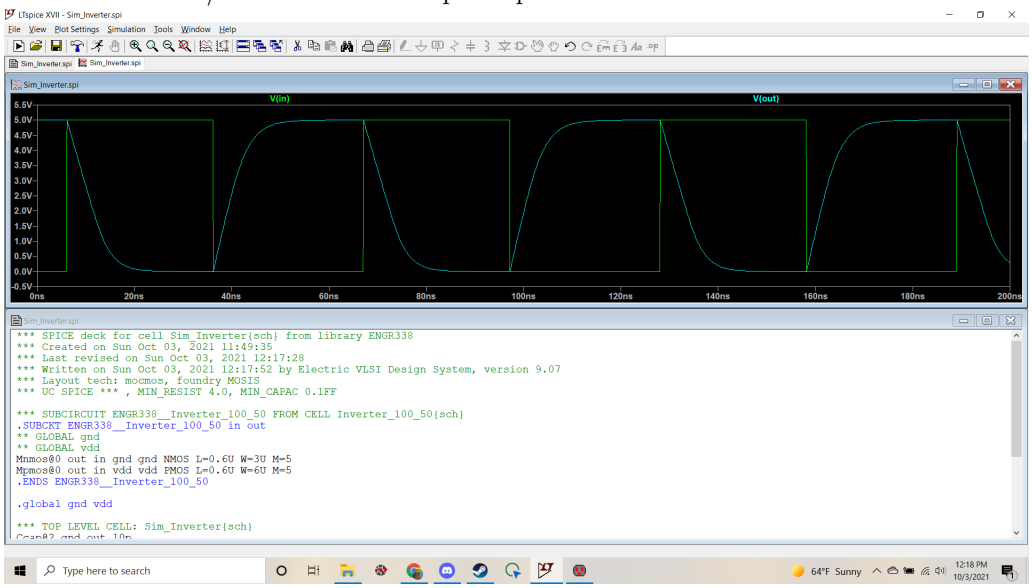
100/50 Inverter with 1pF Capacitor



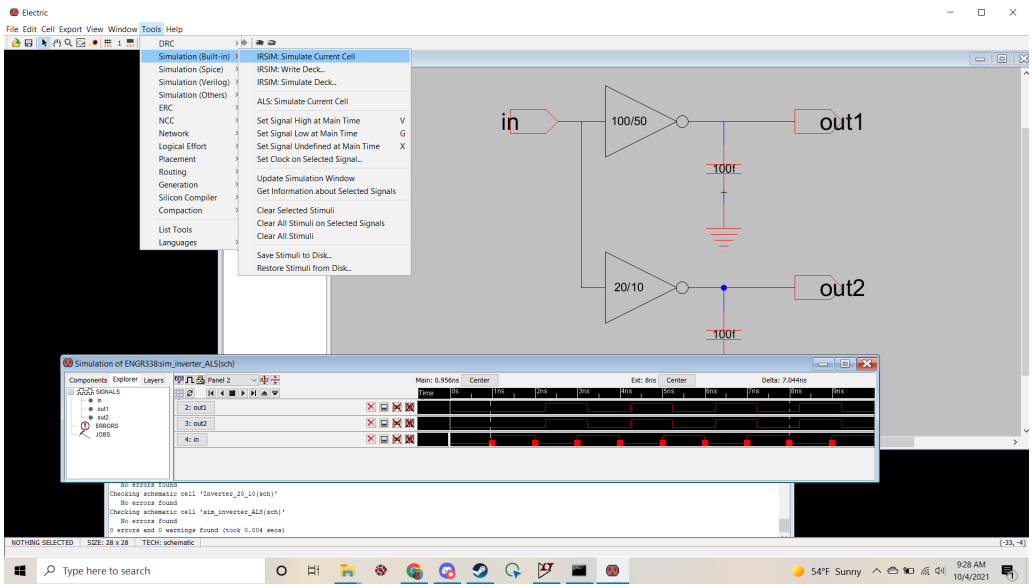
100/50 Inverter with 1pF Capacitor Output



100/50 Inverter with 10pF Capacitor



100/50 Inverter with 10pF Capacitor Output



Electric VLSI IRSIM

4 Discussion

Both inverters worked exactly as they should since all the sims showed the correct output. As we can see, if the inverter is larger and holds more MOSFETS, then it is more responsive with larger capacitances. I personally like to use the LTSpice sims since they are easier to program, manipulate, and implement compared to the IRSIM that Electric VLSI offers, however I am now capable of using both. The construction of these inverters can also be extrapolated out to more complicated CMOS designs such as an NAND gate.