Design an R-2R DAC

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9/12/2021

1 Introduction

DACs (Digital to Analog Converters) are used in all sorts of electrical equipment. Especially those with a sensor of any kind. A R 2R Ladder is a simple way to design and implement a DAC. This paper will go over my process of creating a R 2R ladder DAC in Electric VLSI and LTSpice.

2 Methods

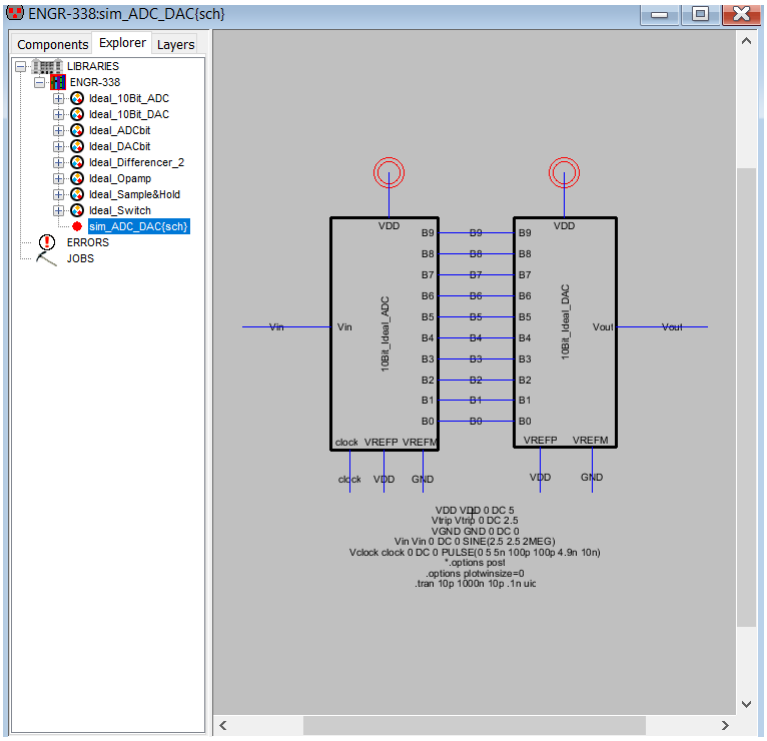
Our first task was to test an ideal DAC that was pre-designed for us in `http://www.yilectronics.com/Courses/ENGR338L_CE/f2021/lab2_DAC/Lab2.html`. This test is designed to make sure all the settings in Electric VLSI are correct and that everything will work for our R 2R Ladder DAC.

Secondly, we design our R 2R Ladder in Elecric VLSI and test it's output in LTSpice. We expect it to look similar to the ideal DAC from our first task.

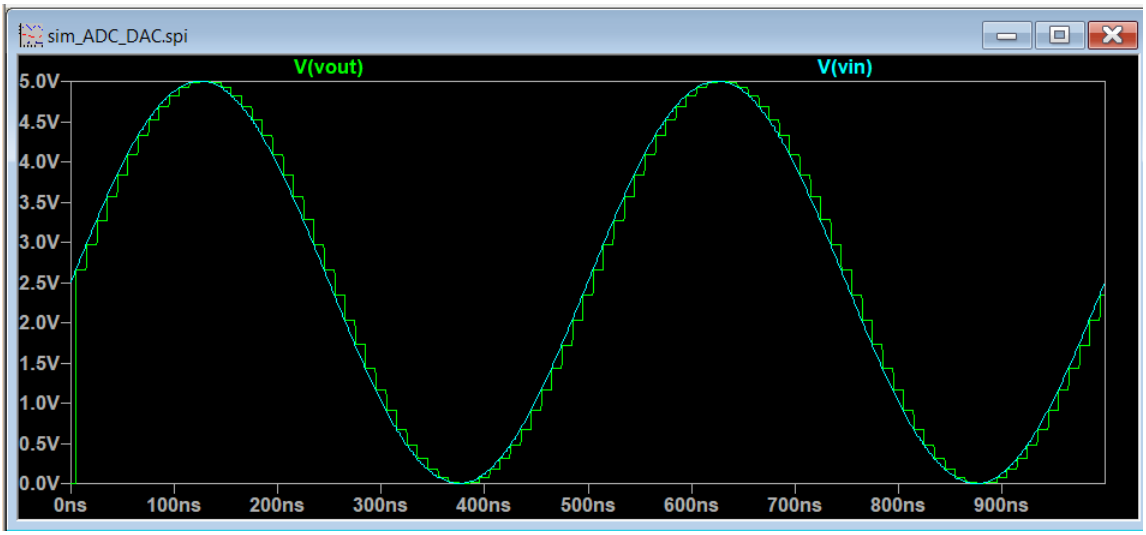
Lastly, we ground all of our DAC's pins except B9 to test our time delay. We expect time delay in the simulation to be nearly equivalent to the time delay equation $.7RC$ where R is the Thevenin Equivalent resistance of B9 and C is the load capacitor of 10pF.

3 Results

3.1 Task 1

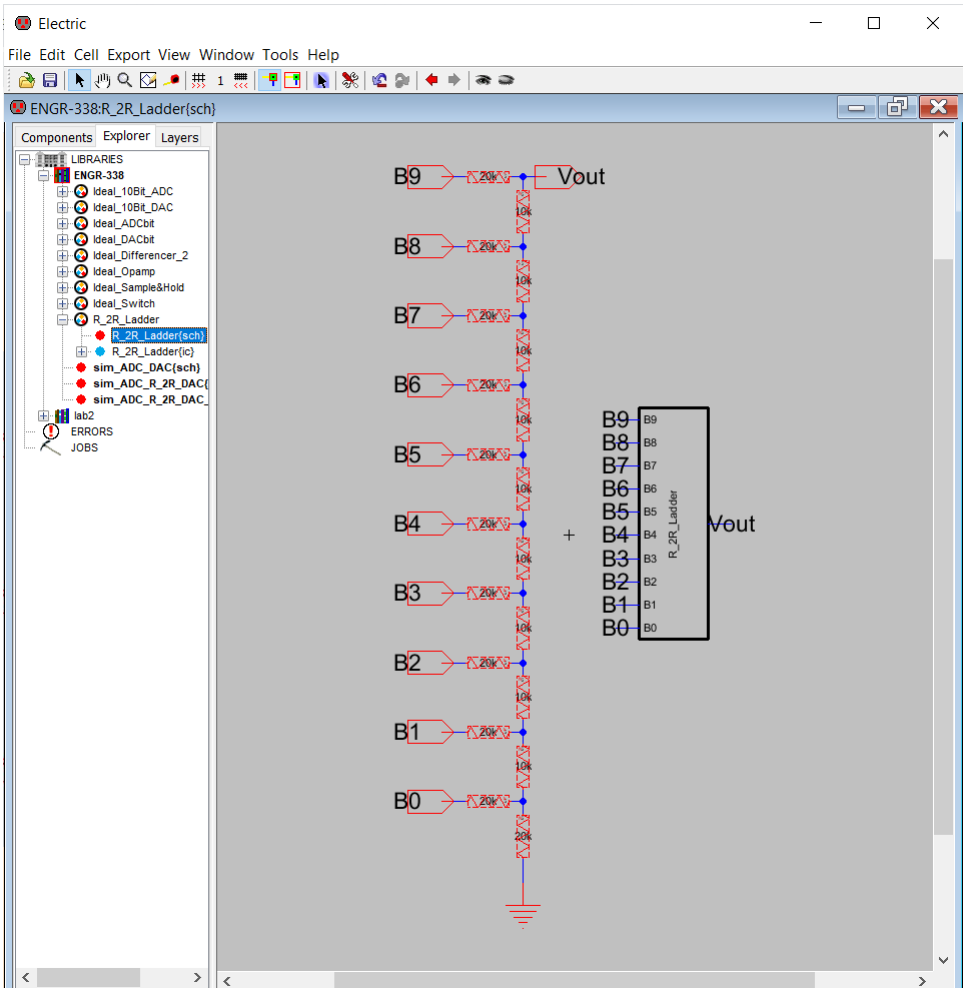


Ideal ADC and DAC Connections

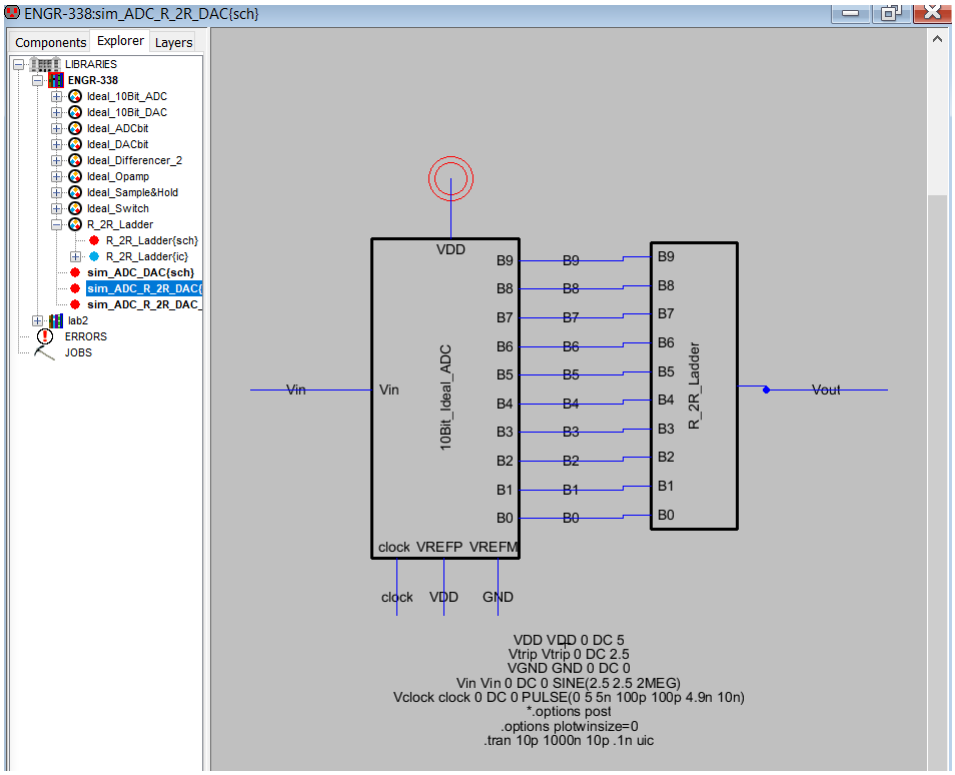


Ideal ADC(Blue) and DAC(Green)

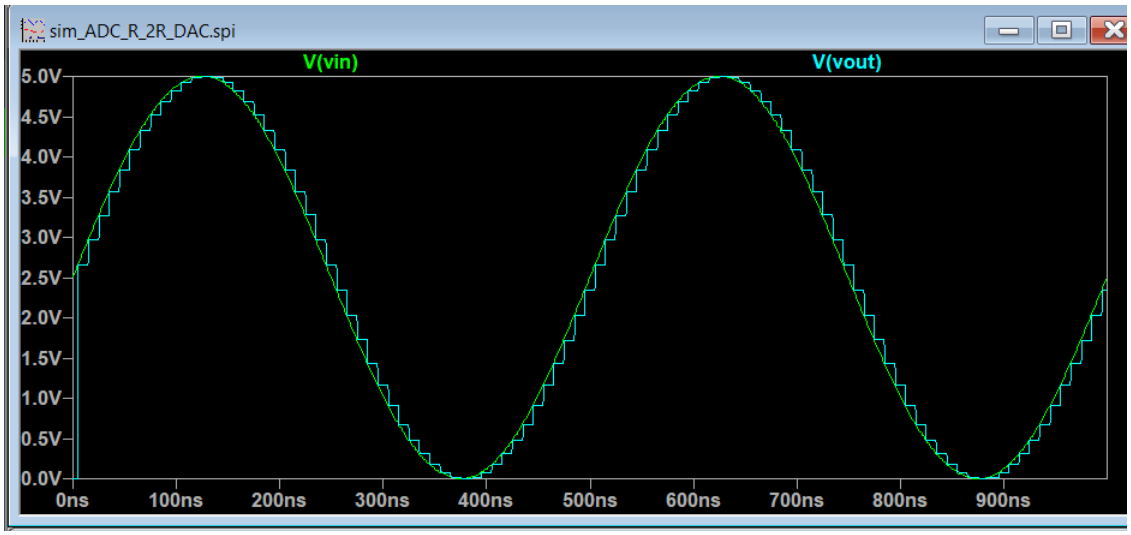
3.2 Task 2



R 2R Ladder DAC

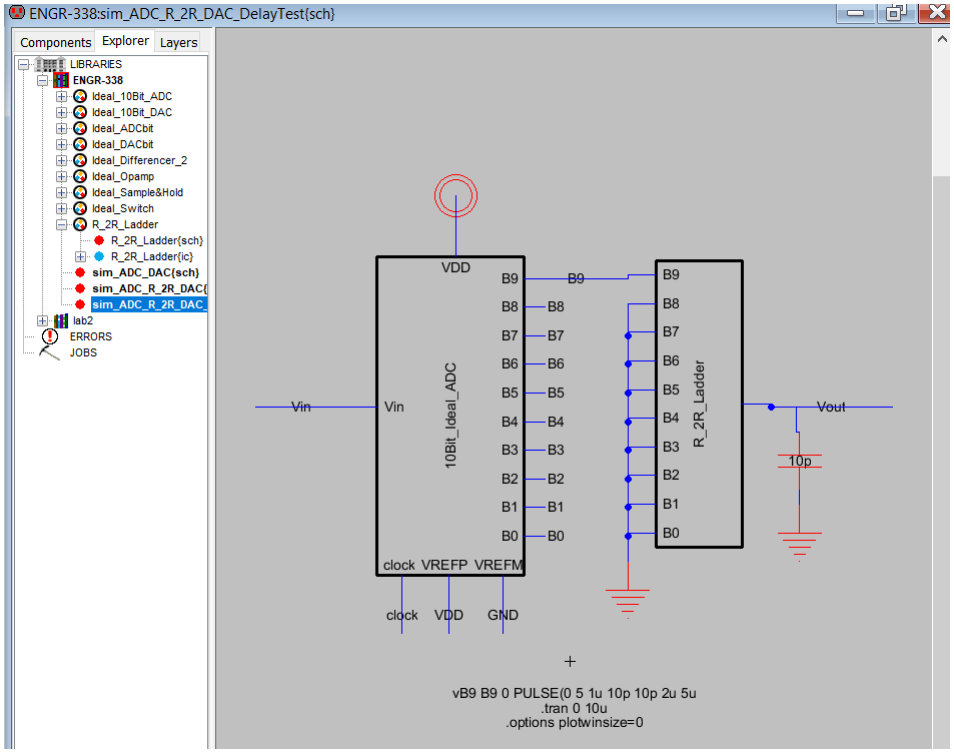


ADC and R 2R Ladder DAC Connections

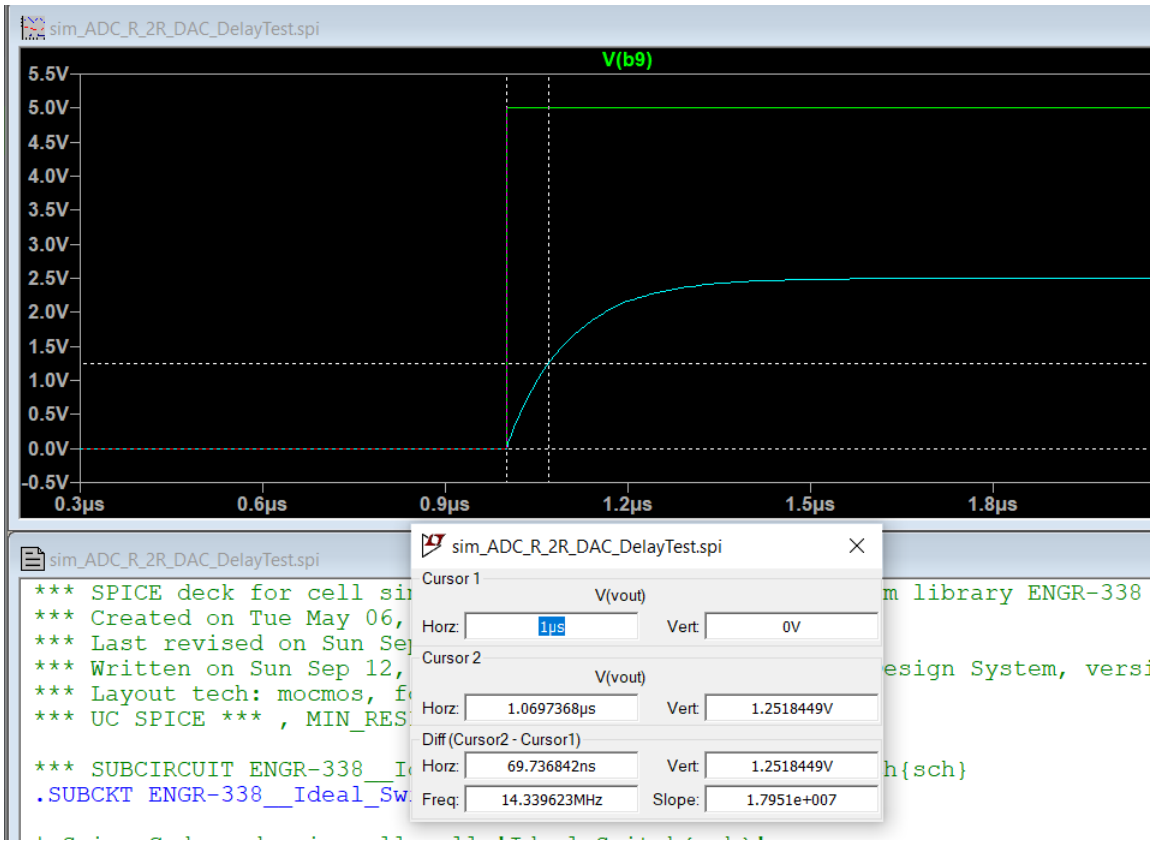


ADC(Green) and R 2R Ladder DAC(Blue)

3.3 Task 3



Time Delay Test for ACD to DAC Connections



Time Delay Results: 70ns

$$R = Rth = (20k\Omega^{-1} + 20k\Omega^{-1})^{-1} = 10k\Omega$$

$$C = C_{load} = 10pF$$

$$.7RC = .7 * 10k * 10p = 70ns$$

4 Discussion

For task 1, we know that everything worked correctly since Vout came out to to approximate Vin by stepping alongside Vin. Task 2 was successful because the Vout for that DAC closely resembled the ideal DAC from task 1. Finally, task 3 was successful since the calculated time delay matched the simulated time delay nearly perfectly. We know to check for the time delay at 1.25V is because Vth is 2.5V and half of 2.5 will give us the time delay.