An 8-bit SAR ADC

Calvin Reese
cjreese@fortlewis.edu

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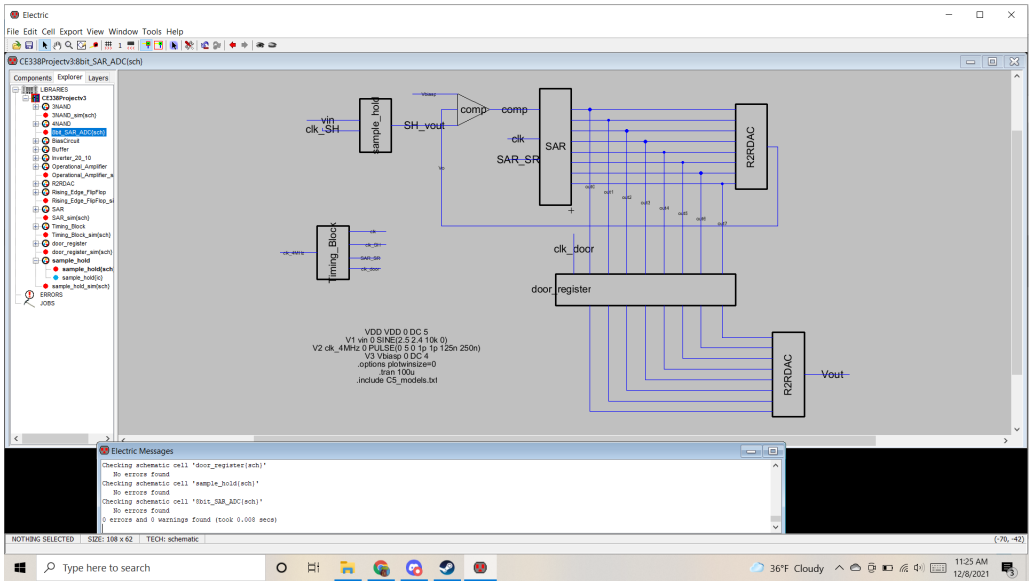
1 Introduction

Most digital circuits require the ability to recognise an analog input. Whether it be a sensor or otherwise, an analog to digital converter (ADC) is required for our digital systems to recognise and work with these analog signals. In this paper, I will go over the electronics required make an ADC.

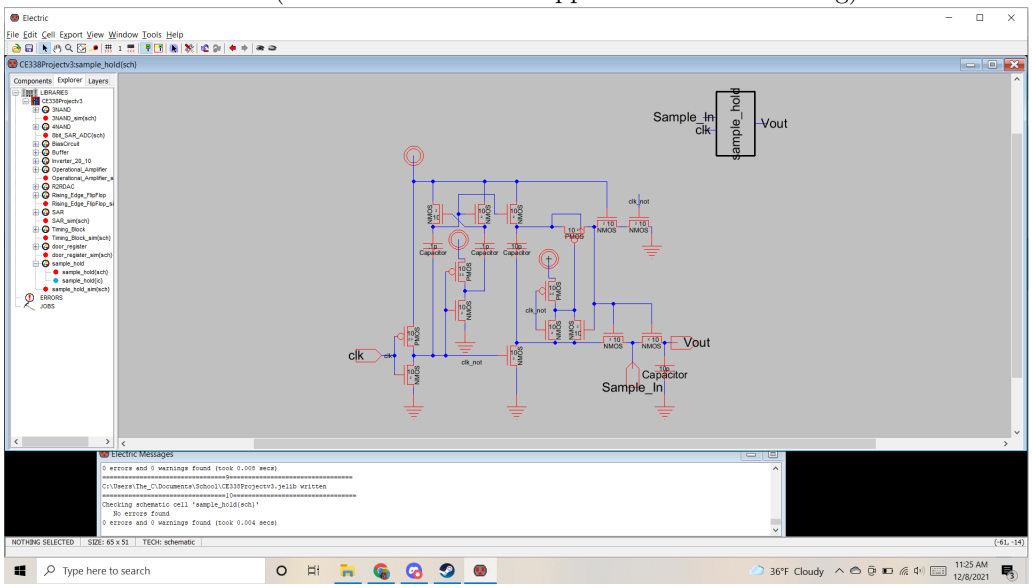
2 Materials and Methods

The instructions for this came from the `http://www.yilectronics.com/Courses/ENGR338_CE/f2021/proj/proj.html` and `http://yilectronics.com/Tutorials/ElectricVLSI_Tutorials/Tutorial_5/ElectricVLSI_Tutorial5.html`.

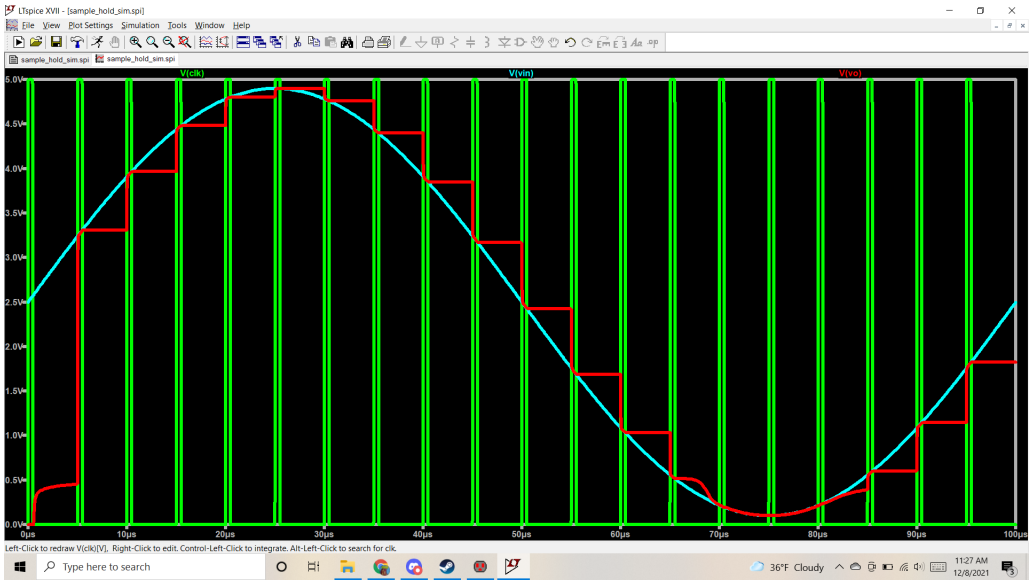
3 Results



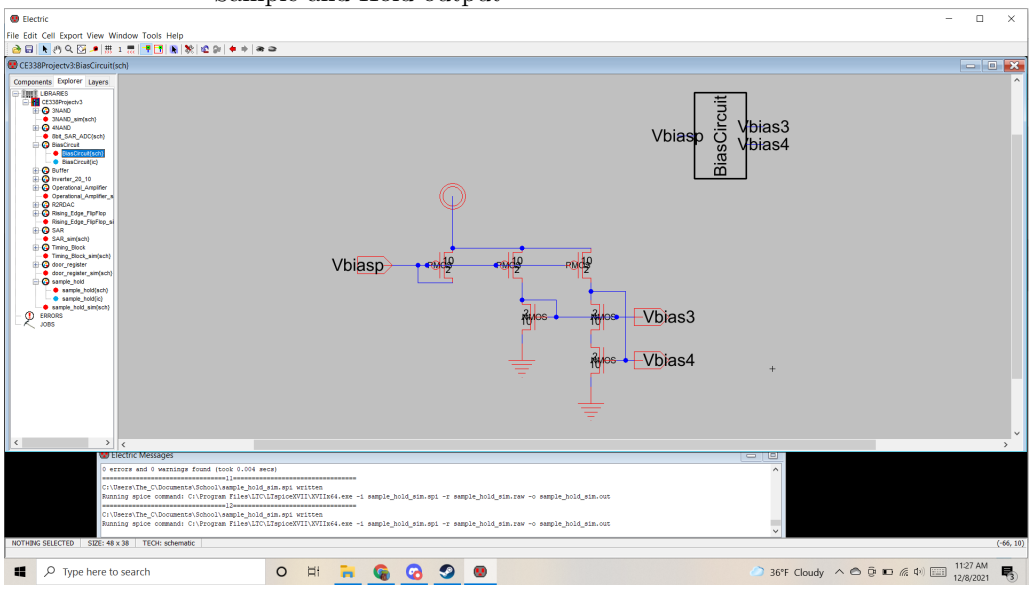
Full ADC Schematic(note this DRC Check applies to all the following)



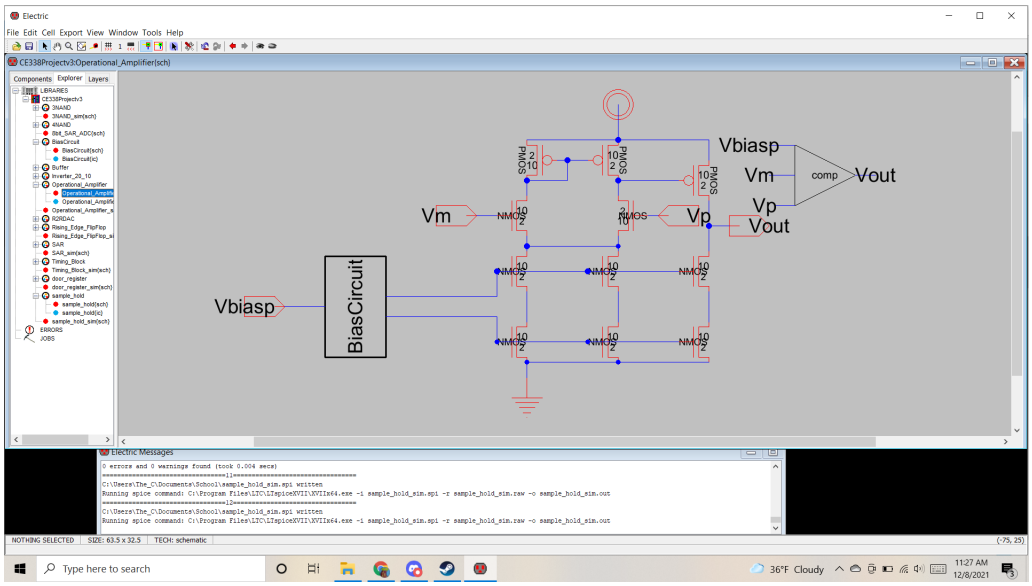
Sample and Hold Schematic



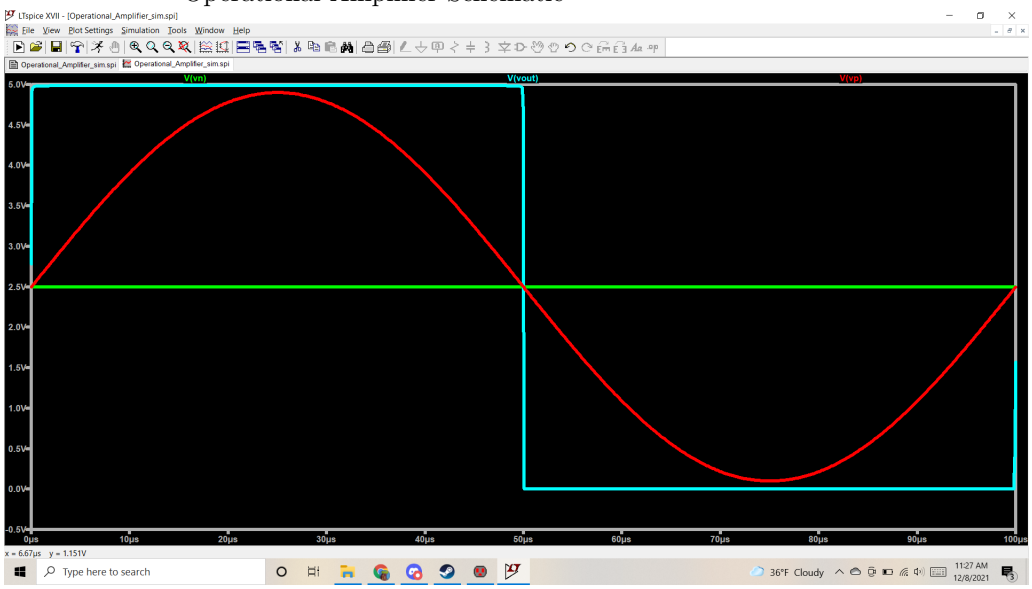
Sample and Hold output



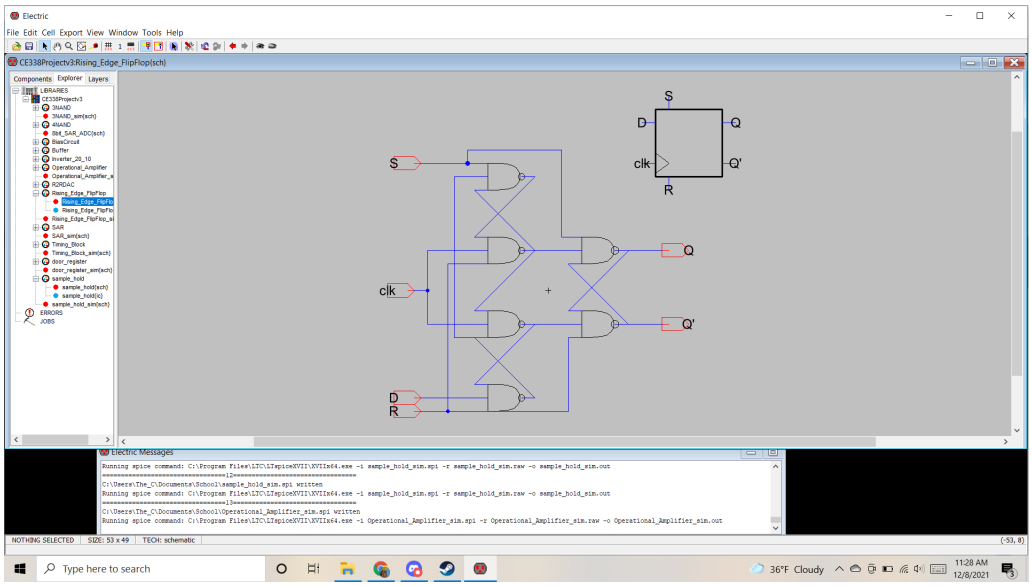
Bias Circuit for Op Amp Schematic



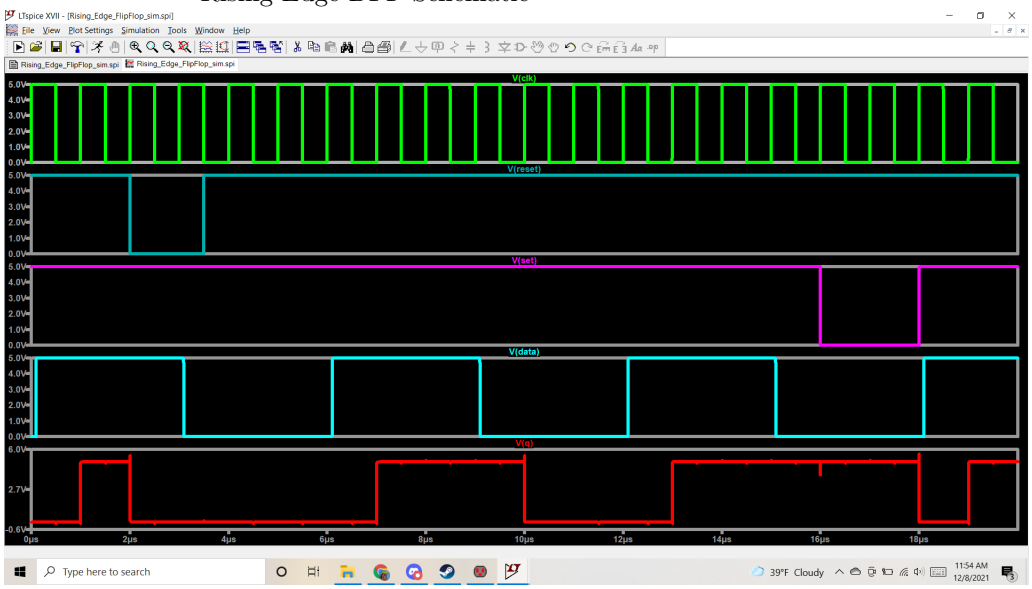
Operational Amplifier Schematic



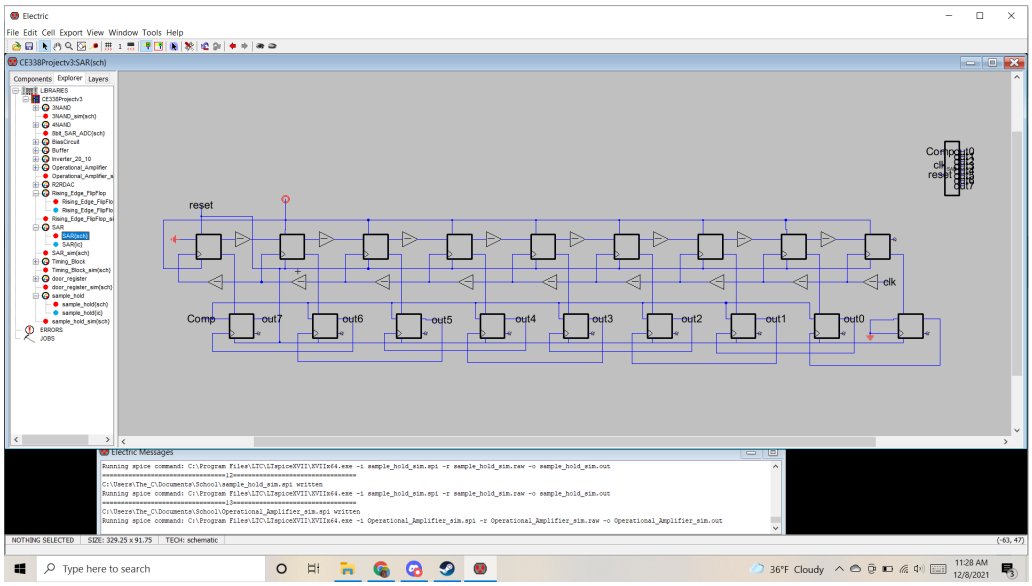
Operational Amplifier Output



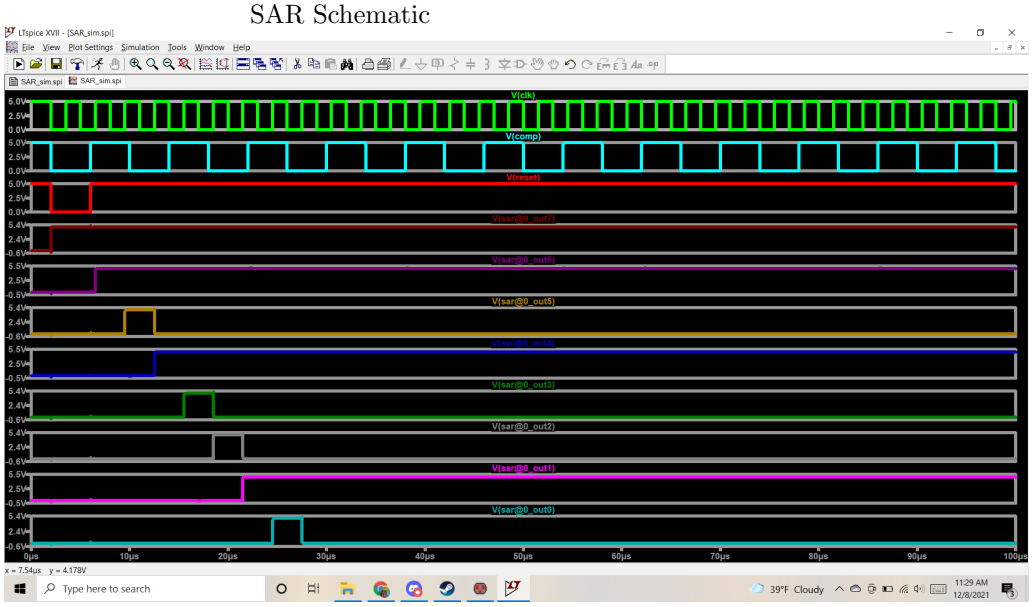
Rising Edge DFF Schematic



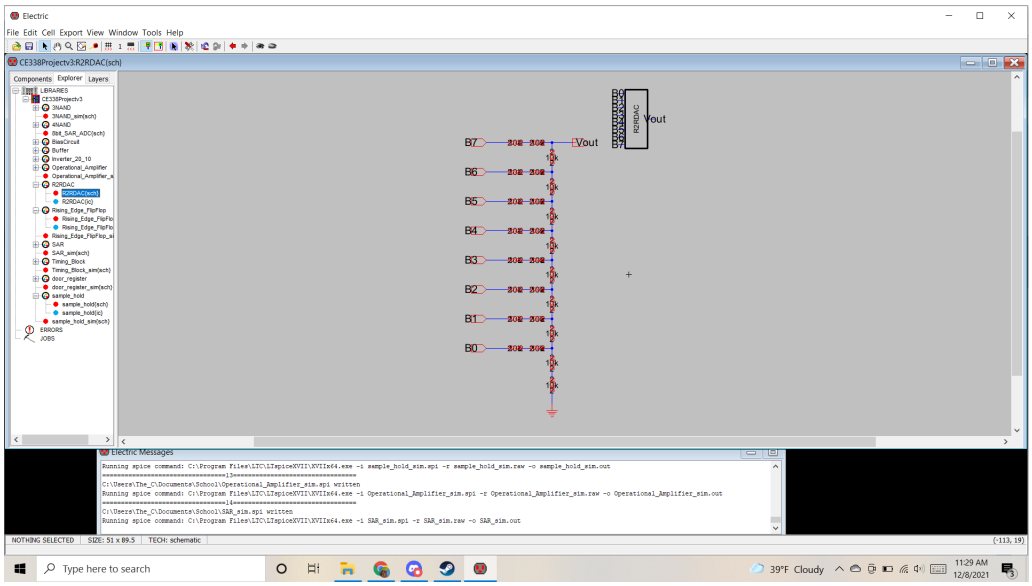
Rising Edge DFF Output



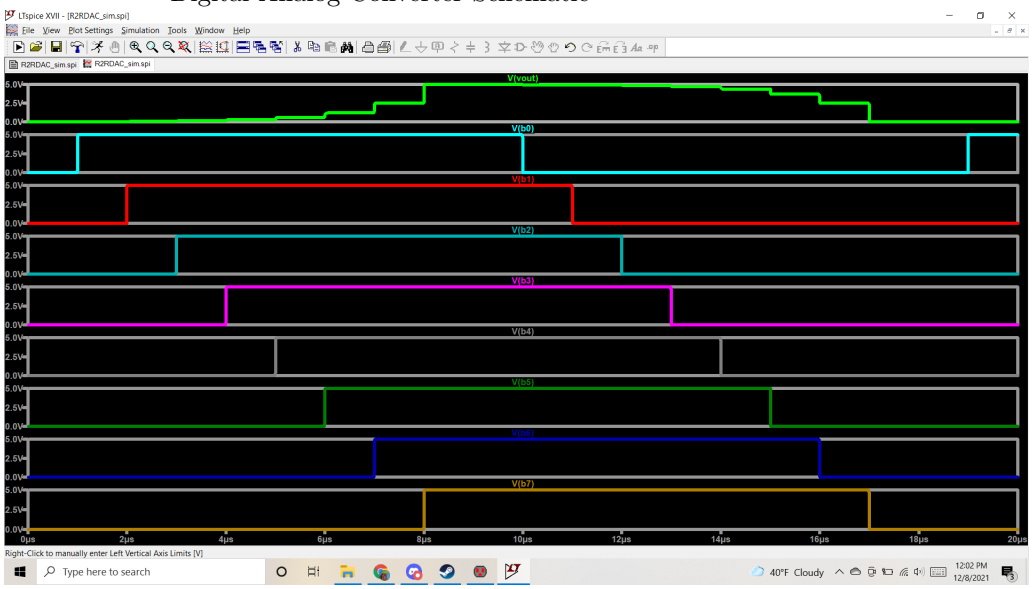
SAR Schematic



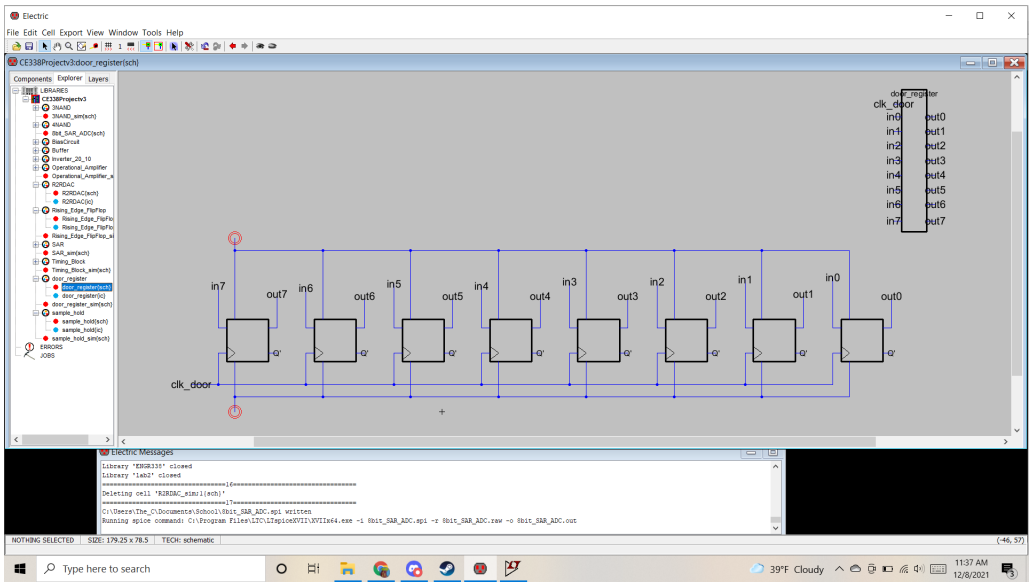
SAR Output



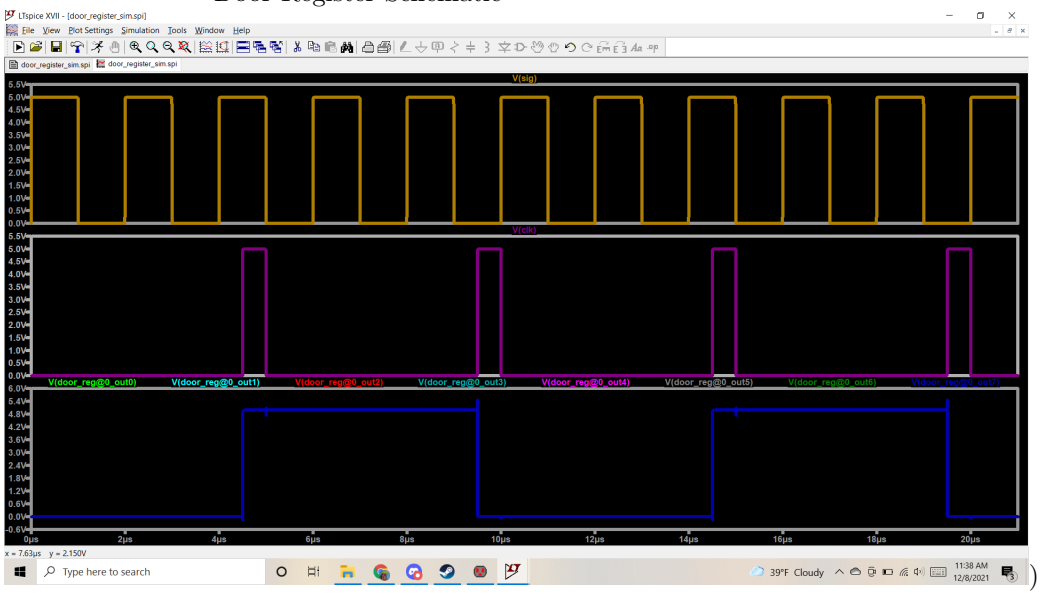
Digital Analog Converter Schematic



DAC Output



Door Register Schematic



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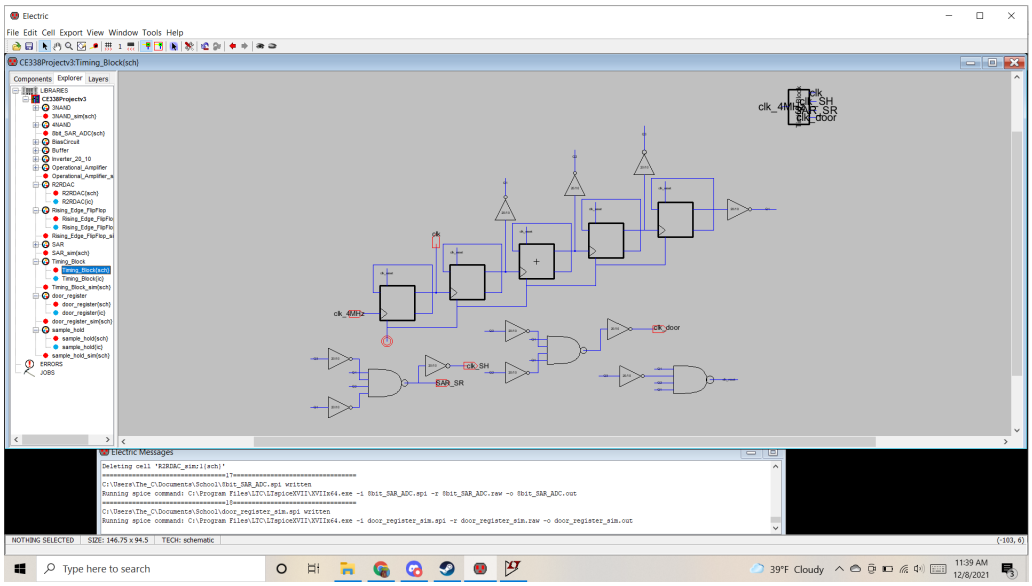
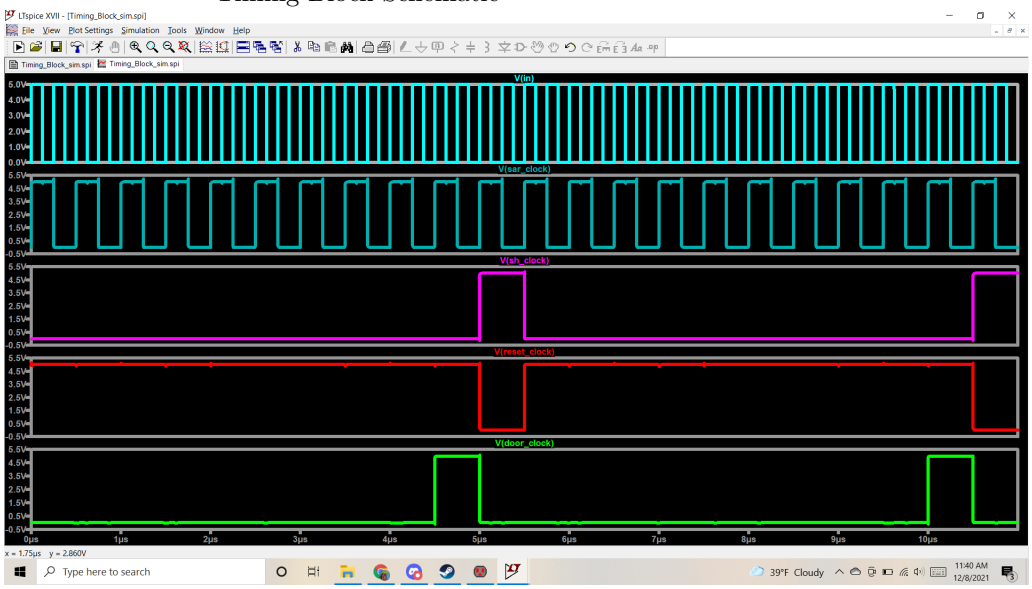
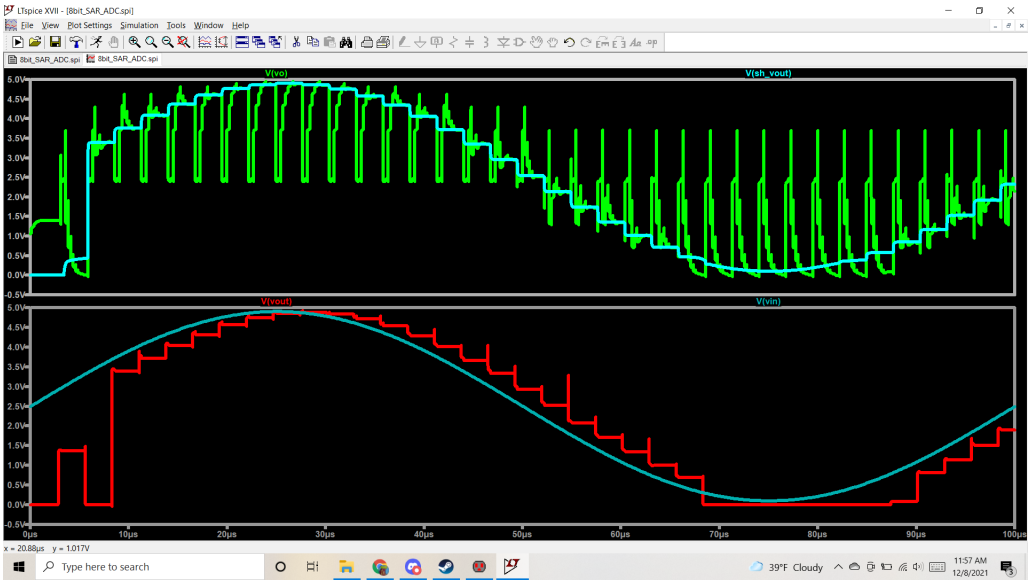
Door Register Output (all inputs sample)



Timing Block Schematic



Timing Block Output



ADC Output

4 Discussion

As seen above, the ACD works rather well after the first iteration of the SAR. With an increase in clock speed, the closer the output will be to the actual input. The green Vo above shows the output of the SAR and OP amp working together to match the output of the sample and hold. Then the door register passes that final value of the SAR to Vout, which the red line next to the sine wave input. The sample and hold does take a second to get the voltage pump working well enough to start accurately holding sample values, which explains the error for the first sample/hold iteration.