State and Output Equations

Calvin Reese
cjreese@fortlewis.edu

3/1/22

1 Introduction

This HW, we worked on designing and testing state and output equations.

2 Materials and Methods

The tutorial for making these examples are in `http://www.yilectronics.com/Courses/CE433/s2022/lectures/week5_sequentialCircuit/week5_sequentialCircuit.html`

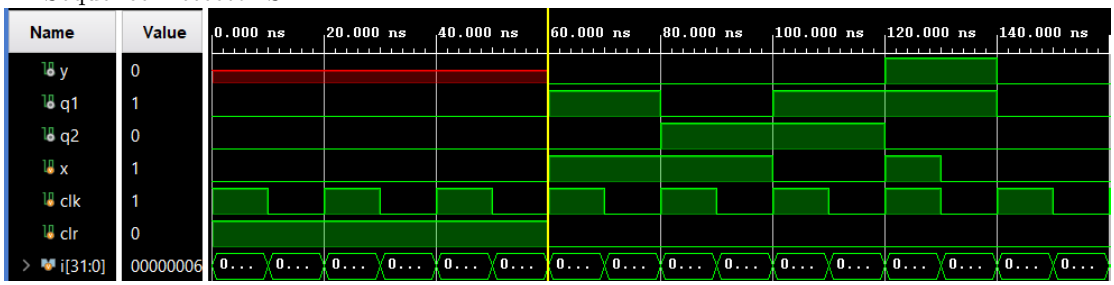
3 Results

3.1 Task 2

Sequence Detector Code

```
23 module sequenceDetector(y,q1,q2,x,clk,clr);
24 input x,clk,clr;
25 output reg y;
26 output reg q1=0;
27 output reg q2=0;
28
29 always @(posedge clk)
30     if(clr==1)
31     begin
32         q1<=1'b0;
33         q2<=1'b0;
34     end
35     else
36     begin
37         q1<=~(q1^q2)*x+(~x*~q1*q2);
38         q2<=(x*q1*~q2)+(~q1*q2);
39         y<=(x*q1*q2);
40     end
41 endmodule
42
43 module sequenceDetector_tb;
44 wire y,q1,q2;
45 reg x=0;
46 reg clk=0;
47 reg clr=1;
48 integer i;
49
50 sequenceDetector UUT(.y(y),.q1(q1),.q2(q2),.x(x),.clk(clk),.clr(clr));
51 initial begin
52     for(i=0;i<20;i=i+1)begin
53         clk=~clk;
54         if(i>5&i<10)begin
55             clr=0;
56             x=1;
57         end
58         else if(i==11) x=0;
59         else if(i==12) x=1;
60         else x=0;
61         #10;
62     end
63 end
64 endmodule
```

Sequence Detector Sim

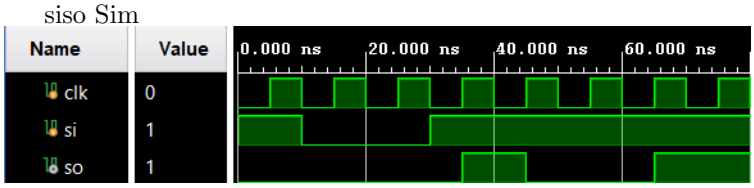


3.2 Task 3

siso Code

```
21 module siso(clk,si,so);
22 input clk,si;
23 output so;
24 reg [3:0] q=0;
25 always @(posedge clk)
26 begin
27     q[3]<=si;
28     q[2]<=q[3];
29     q[1]<=q[2];
30     q[0]<=q[1];
31 end
32 assign  so=q[0];
33 endmodule
34
35 module siso_tb;
36 reg clk;
37 reg si;
38 wire so;
39 siso U(.clk(clk),.si(si),.so(so));
40 initial begin
41 clk=0;
42 si=1;
43 #10
44 si=0;
45 #10
46 si=0;
47 #10
48 si=1;
49 end
50 always #5 clk=~clk;
51 endmodule
```

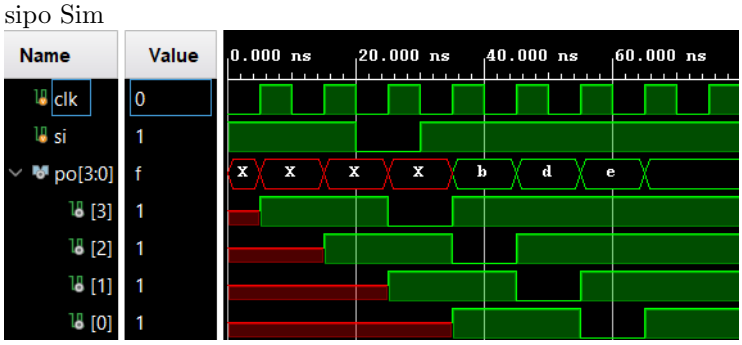
siso Sim



sipo Code

```
55 module sipo(clk,si,po);
56 input clk,si;
57 output [3:0] po;
58 reg [3:0] tmp;
59 always @(posedge clk)
60 begin
61     tmp={si,tmp[3:1]};
62 end
63 assign  po=tmp;
64 endmodule
65
66 module sipo_tb;
67 reg clk;
68 reg si;
69 wire [3:0] po;
70 sipo U(.clk(clk),.si(si),.po(po));
71 initial begin
72 clk=0;
73 si=1;
74 #10
75 si=1;
76 #10
77 si=0;
78 #10
79 si=1;
80 end
81 always #5 clk=~clk;
82 endmodule
```

sipo Sim



piso Code

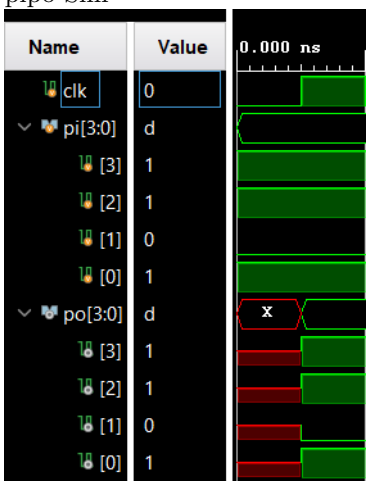
```
86 module piso(clk,pi,load,so);
87 input clk,load;
88 input [3:0] pi;
89 output reg so;
90 reg [3:0] tmp;
91 always @(posedge clk)
92 begin
93     if(load) tmp<=pi;
94     else
95     begin
96         so<=tmp[0];
97         tmp<={1'b0,tmp[3:1]};
98     end
99 end
100 assign  po=tmp;
101 endmodule
102
103 module piso_tb;
104 reg clk;
105 reg [3:0] pi=4'b1101;
106 wire so;
107 reg load;
108 piso U(.clk(clk),.pi(pi),.so(so),.load(load));
109 initial begin
110     clk=0;
111     load=1;
112     #10;
113     load=0;
114 end
115 always #5 clk=~clk;
116 endmodule
```

piso Sim

pipo Code

```
120 module pipo(clk,pi,po);
121 input clk;
122 input [3:0] pi;
123 output reg [3:0] po;
124 always @(posedge clk)
125 begin
126     po=pi;
127 end
128 endmodule
129
130 module pipo_tb;
131 reg clk;
132 reg [3:0] pi=4'b1101;
133 wire [3:0] po;
134 pipo U(.clk(clk),.pi(pi),.po(po));
135 initial begin
136     clk=0;
137     #10;
138 end
139 always #5 clk=~clk;
140 endmodule
```

pipo Sim

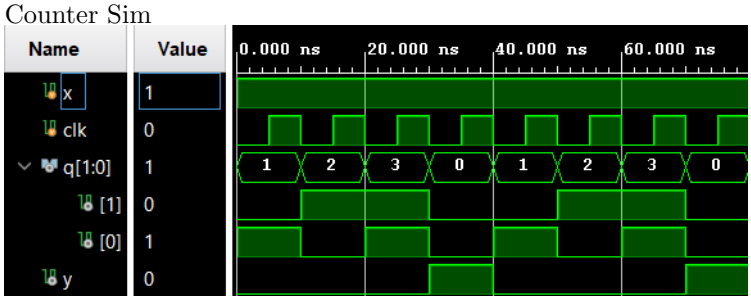


3.3 Task 4

Counter Code

```
23 module Counter(x,clk,q,y);
24 input x,clk;
25
26 output reg [1:0] q;
27 output reg y;
28
29 initial begin
30 q<=1'b00;
31 y<=1'b0;
32 end
33 always @(negedge clk)
34 if (x==1) {y,q} <= q+1'b1;
35 endmodule
36
37 module Counter_tb;
38 reg x,clk;
39 wire [1:0] q;
40 wire y;
41 Counter U(.clk(clk),.x(x),.q(q),.y(y));
42 initial begin
43 clk<=1'b0;
44 x<=1'b1;
45 end
46 always #5 clk=~clk;
47 endmodule
```

Counter Sim

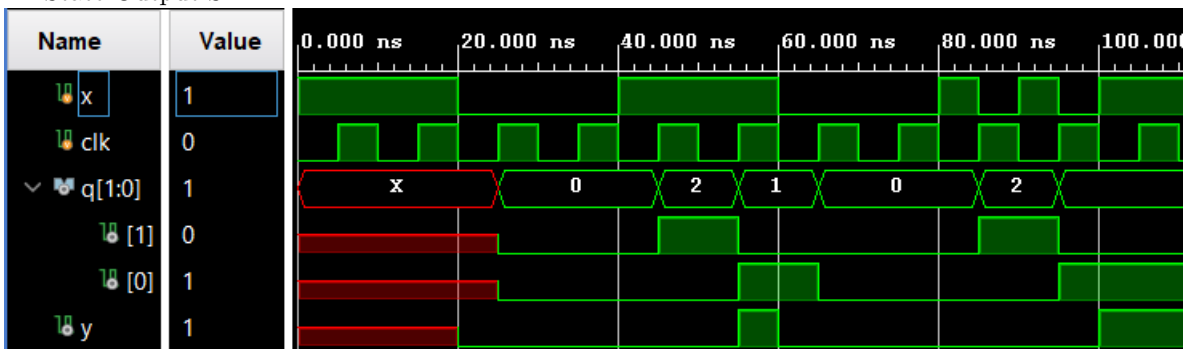


3.4 Task 5

State Output Code

```
23 module stateOutput(clk,q,x,z);
24 input x,clk;
25 output z;
26 output reg [1:0] q;
27 assign z=q[0]&x;
28 always @(posedge clk)
29 begin
30     q[0]<=q[0]&x|q[1]&x;
31     q[1]<=~q[0]&x&~q[1];
32 end
33 endmodule
34
35 module stateOutput_tb;
36 reg x,clk;
37 wire [1:0] q;
38 wire y;
39 stateOutput U(.clk(clk),.q(q),.x(x),.z(y));
40 initial begin
41 clk<=1'b0;
42 x<=1'b1;
43 #20;
44 x<=1'b0;
45 #20;
46 x<=1'b1;
47 #20;
48 x<=1'b0;
49 #20;
50 x<=1'b1;
51 #5;
52 x<=1'b0;
53 #5;
54 x<=1'b1;
55 #5;
56 x<=1'b0;
57 #5;
58 x<=1'b1;
59 end
60 always #5 clk=~clk;
```

State Output Sim



4 Discussion

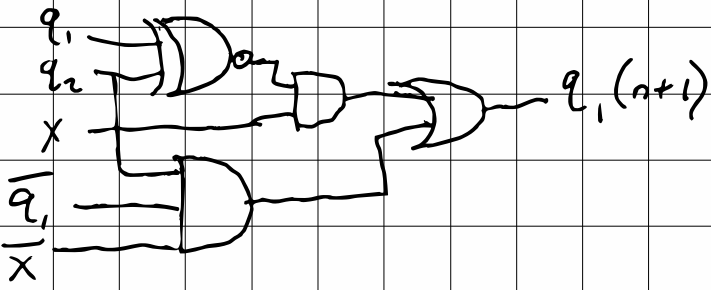
All of this was fairly simple just to follow your tutorial. I had no trouble figuring out the problems. The only difference might be that the siso code and output is based on 1001 instead of 1101.

Task 1

$q_1(n+1)$

x \ q_1q_2	00	01	11	10
0	0	1	0	0
1	1	0	1	0

$$x \cdot \overline{(q_1 \oplus q_2)} + \overline{x} \cdot \overline{q_1} \cdot q_2$$



y

x \ q_1q_2	00	01	11	10
0	0	0	0	0
1	0	0	1	0