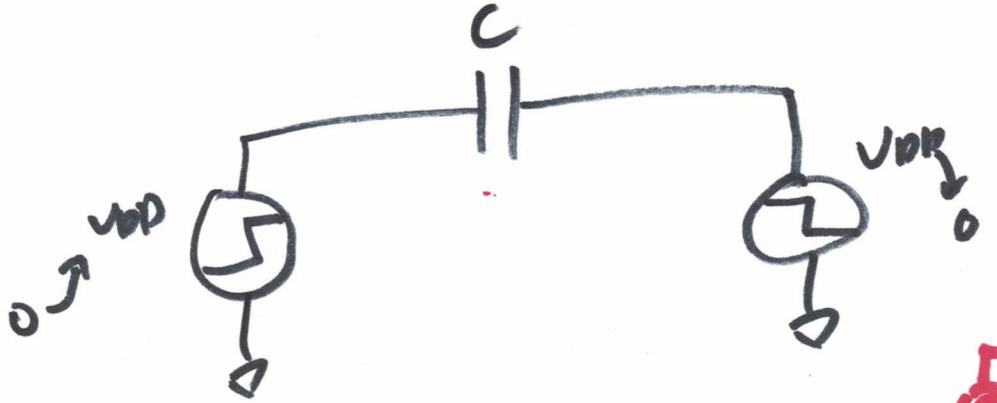
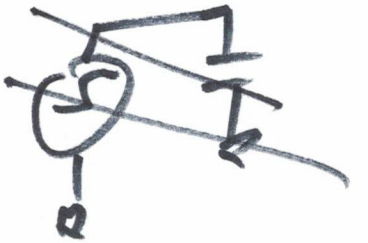
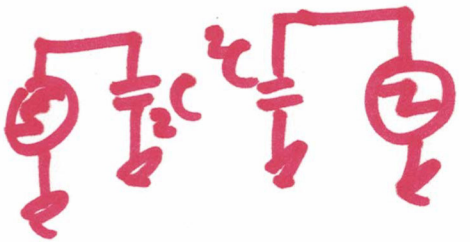
Miller Effect

When circuit has a voltage gain, the input capacitance is larger than the physical capacitance.



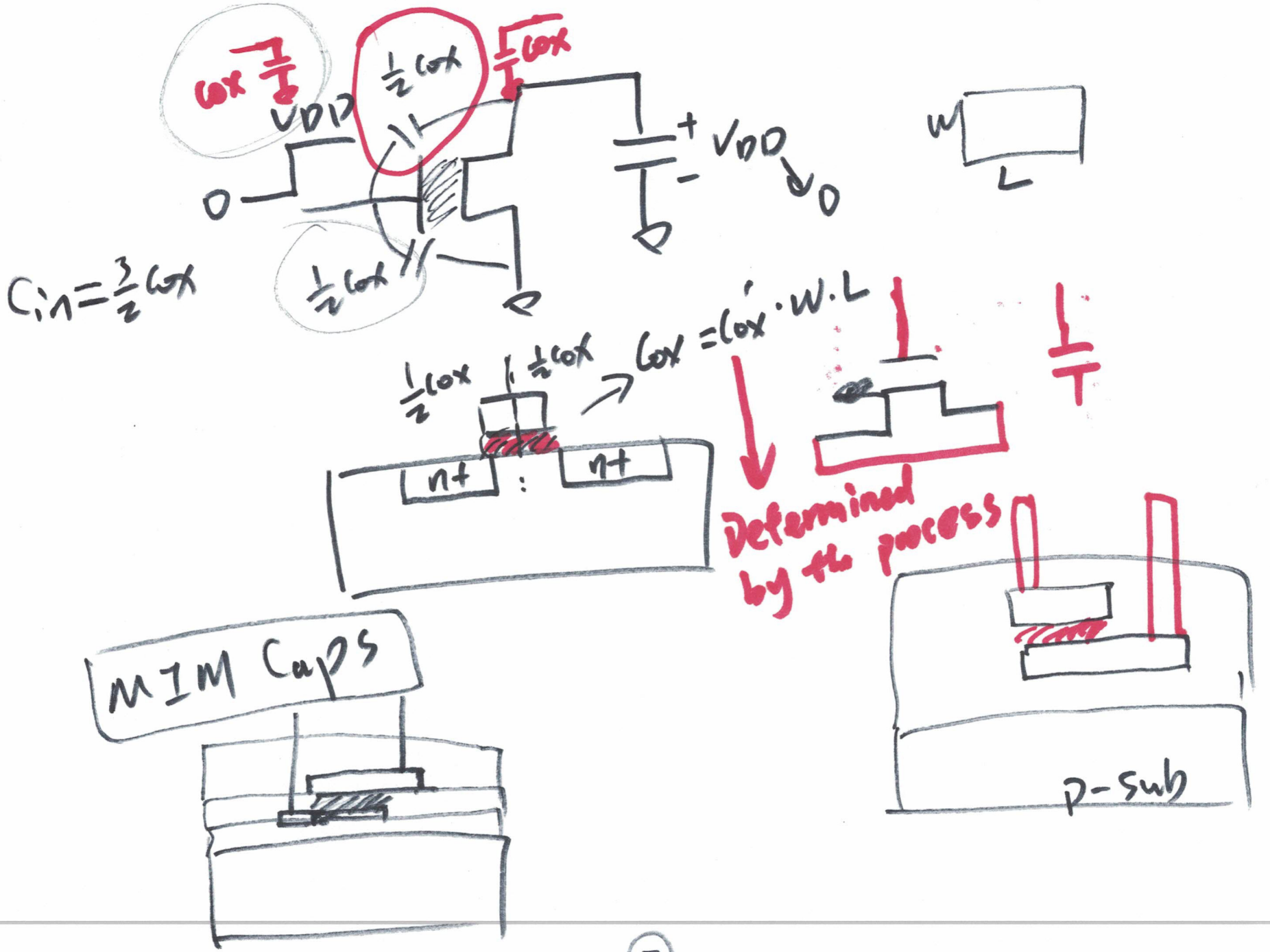


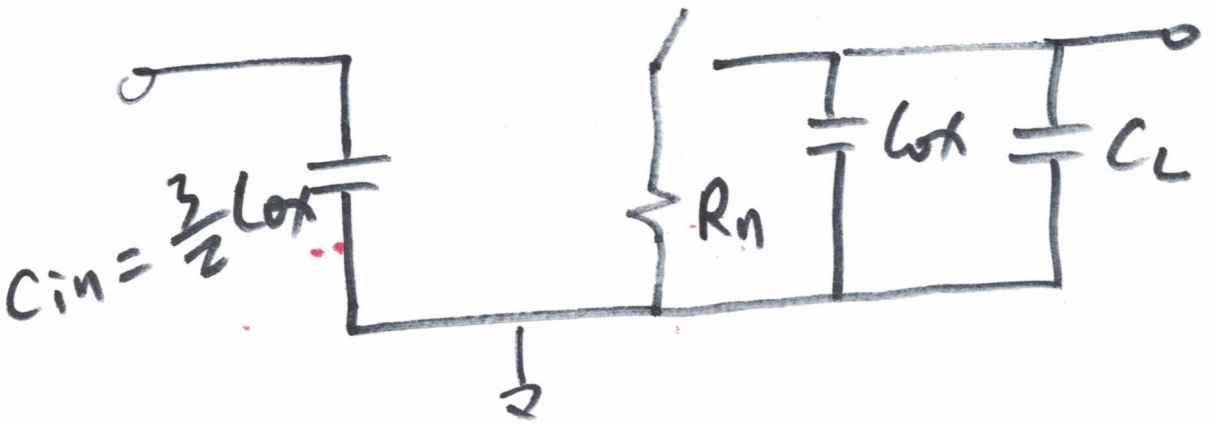


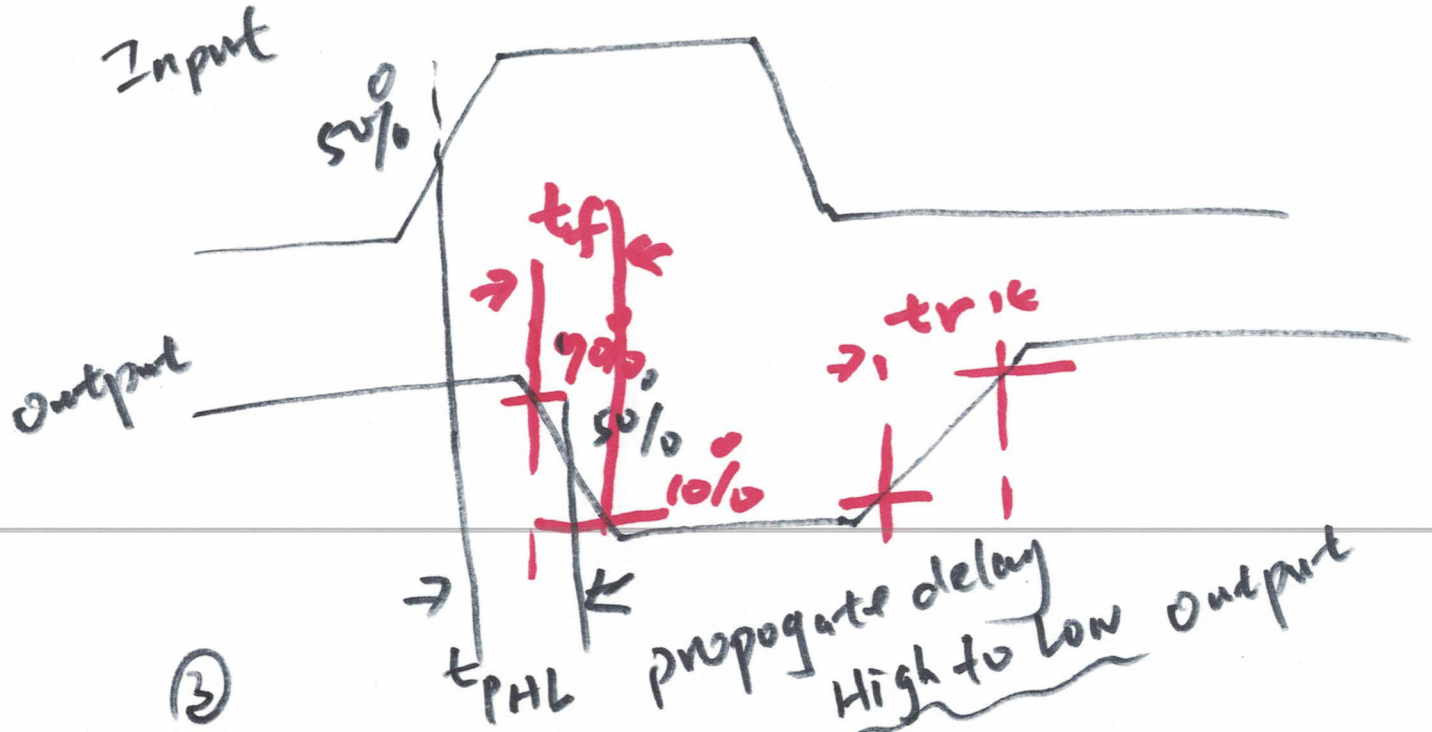
$$\Delta V = 2V_{DD}$$

$$\Delta Q = 2V_{DD} \cdot C$$

$$C_{eff} = \frac{\Delta Q}{V_{DD}} = \frac{2V_{DD} \cdot C}{V_{DD}} = 2C$$


Cox 3/2
VDD
1/2 Cox
1/2 Cox
0
1/2 Cox
Cin = 3/2 Cox
+
VDD → 0
-
W
L
1/2 Cox
1/2 Cox
Cox = Cox' · W · L
n+
n+
Determined by the process
MIM Caps
p-sub

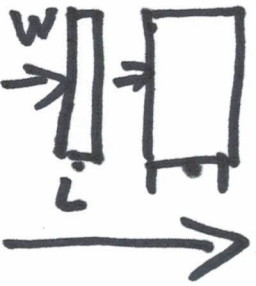

Cin = 3/2 Cox
Rn
Cox
CL

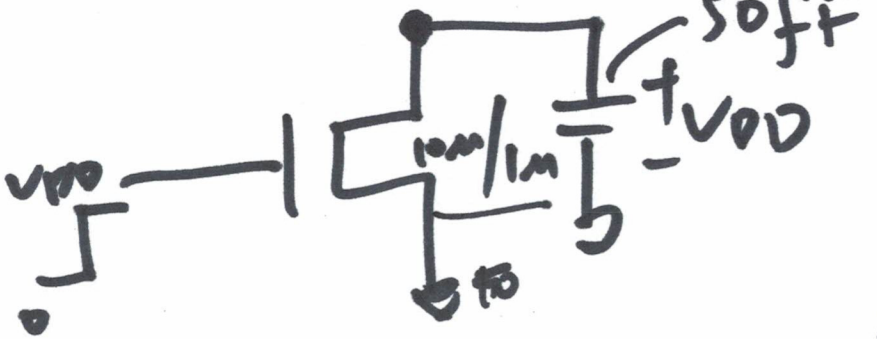

Input
50%
tf
90%
50%
10%
output
tr
tPHL propogate delay
High to Low output

Example P32.

	Sizes	$R_{n,p}$	$C_{oxn,p}$
NMOS	10u/1u	1.5K	17.5fF
PMOS	30u/1u	1.5K	52.5fF

top view



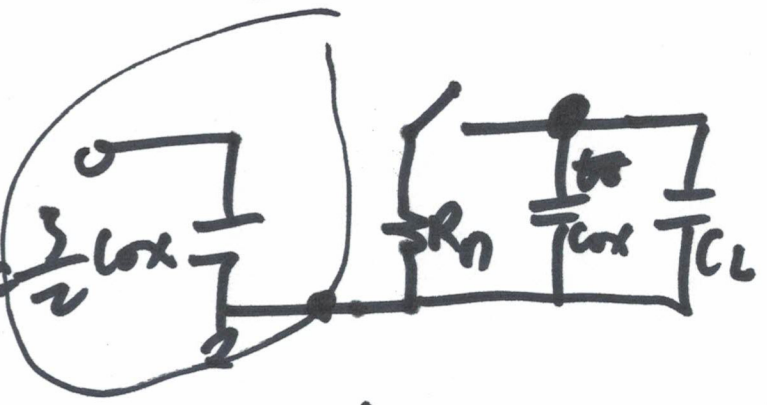


10u/2u

$C_{oxn} = 17.5fF \times 2$

$R_n = 3K$

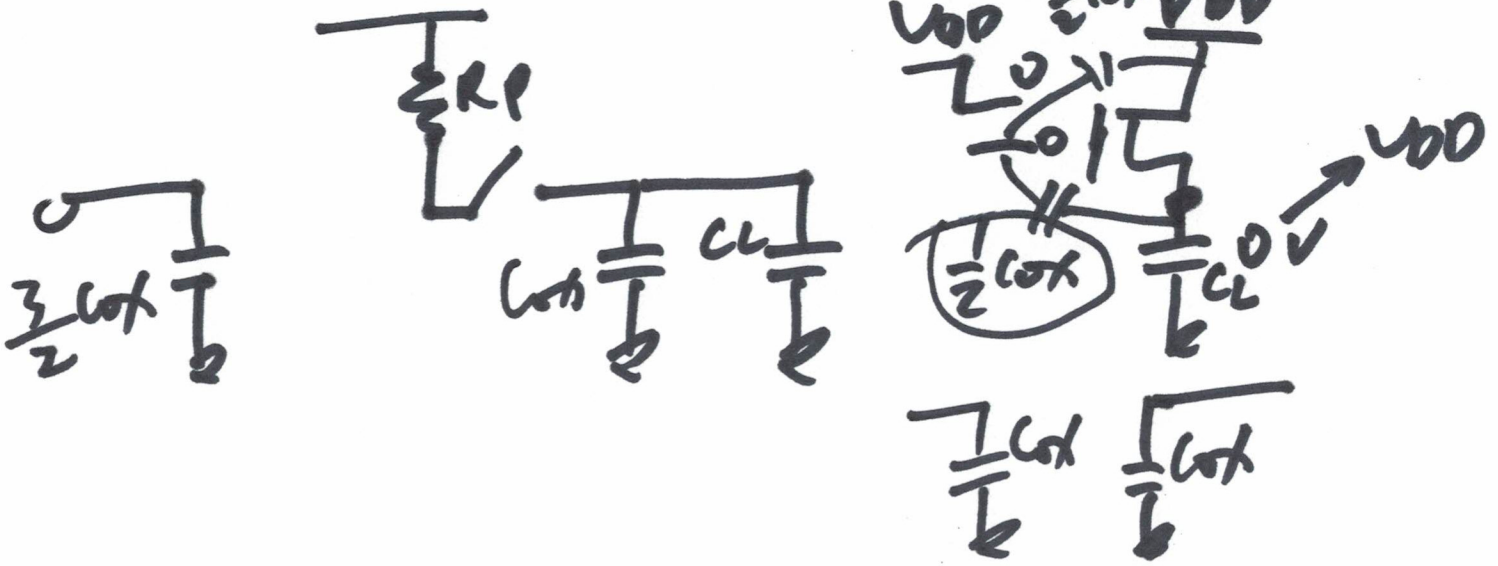
$R = \rho \frac{D}{A}$ $C = \varepsilon \frac{A}{d}$



$C_{in} = \frac{3}{2} C_{ox}$

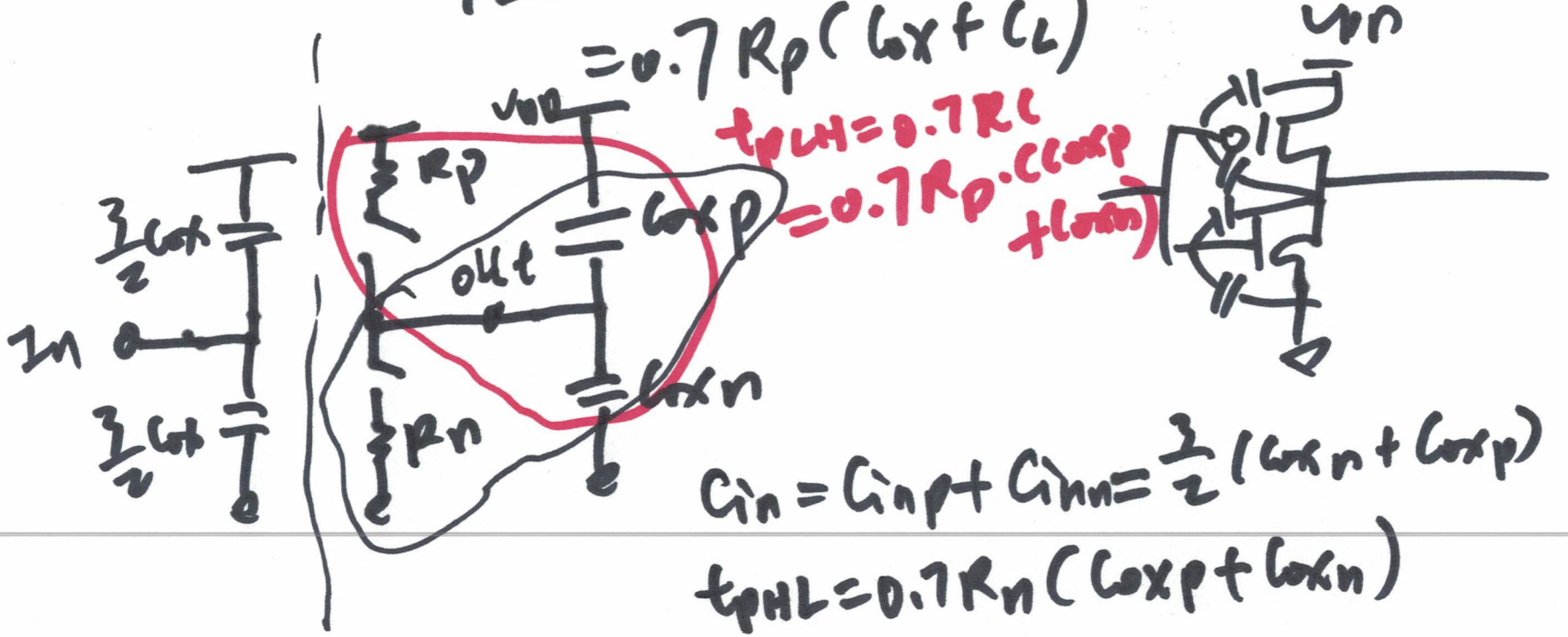
$t_{pHL} = 0.7 \cdot R_n \cdot (C_{ox} + C_L)$

$= 0.7 \cdot 1.5K \cdot (17.5fF + 50fF)$



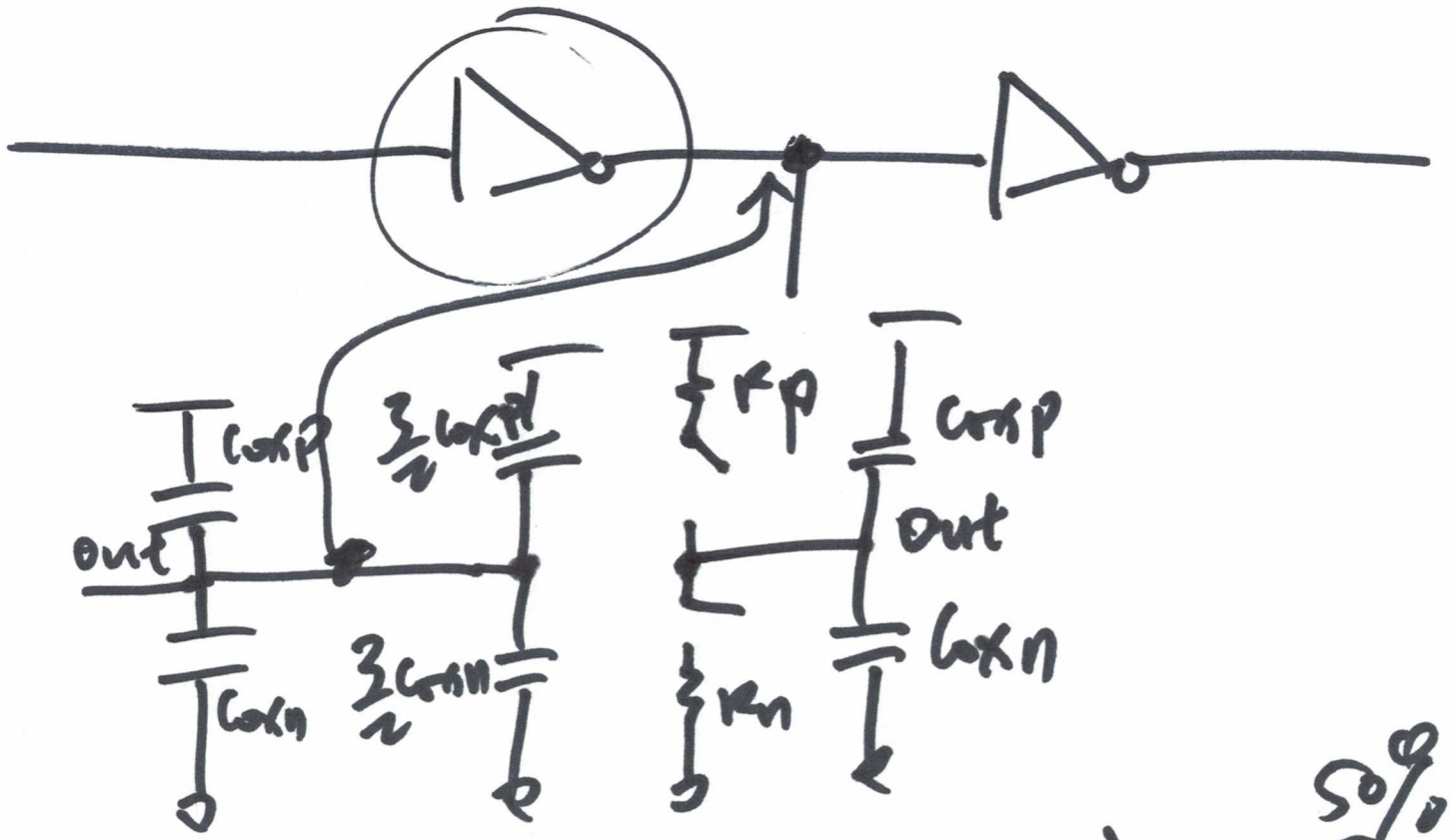
$$t_{PLH} = 0.7RC$$

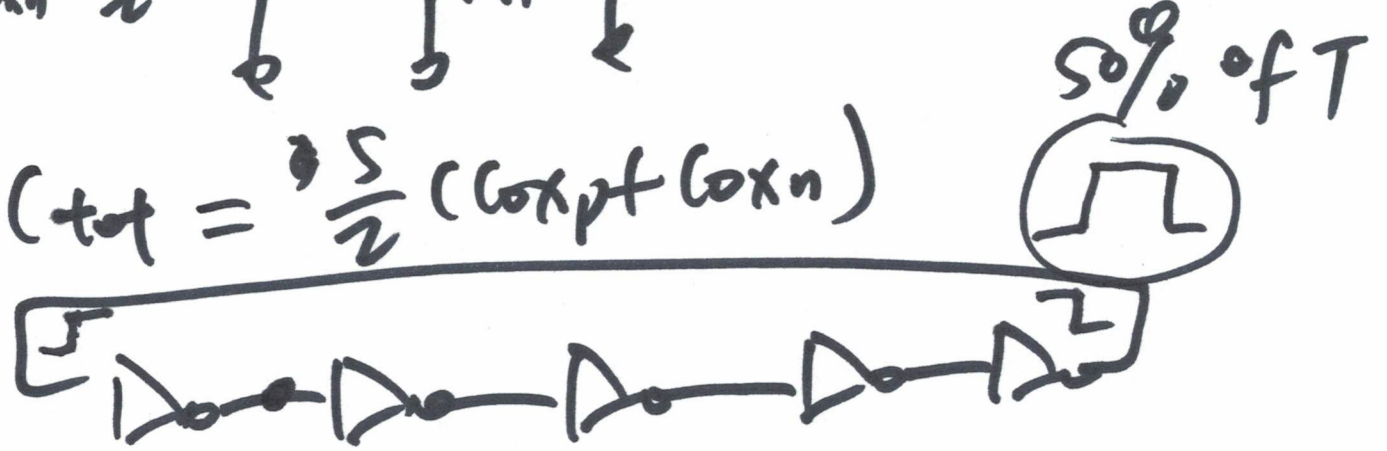
$$= 0.7 R_p (C_{ox} + C_L)$$



$$C_{in} = C_{inp} + C_{inn} = \frac{3}{2}(C_{ox n} + C_{ox p})$$

$$t_{pHL} = 0.7 R_n (C_{oxp} + C_{oxn})$$





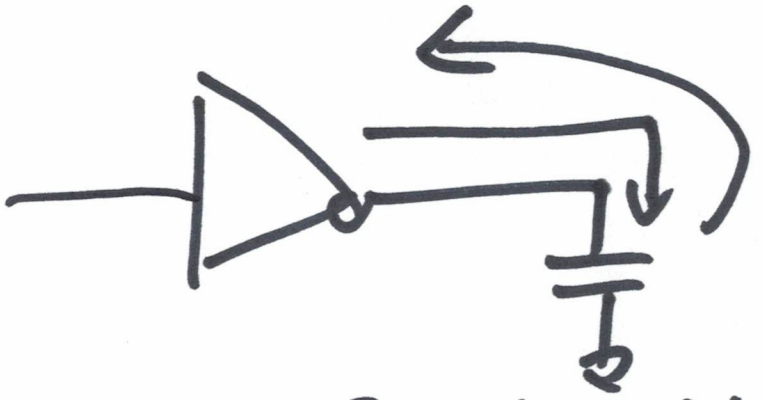
$$(t_{ot} = \frac{5}{2}(C_{oxp} + C_{oxn})$$

$$T = 5t_{pHL} + 5t_{pLH}$$

$$\therefore f = \frac{1}{T} = \frac{1}{5(t_{pHL} + t_{pLH})}$$

(d)

Dynamic Power Dissipation



$$I_{avg} = \frac{Q_{tot}}{T} = \frac{V_{DD} C_{tot}}{T}$$

$$P_{avg} = I_{avg} \cdot V_{DD}$$

$$= \frac{V_{DD}^2 \cdot C_{tot}}{T} = V_{DD}^2 \cdot C_{tot} \cdot f$$