CE338 Digital VLSI Design Spring 2025 Midterm Exam Close-book, close-notes. Calculator is allowed. Wednesday 8 – 8:55 am, 2/19/2025

1. (a) What is the period of input square wave (the PULSE function)? (b) What is the time delay of the output compared to the input? (Derivation is not required). (10 points)

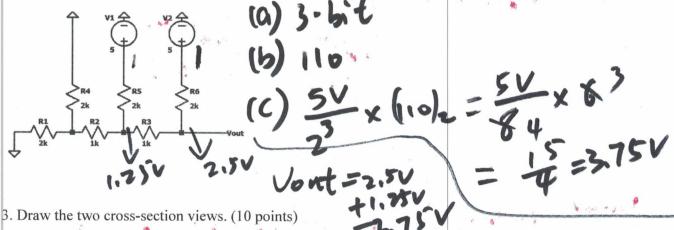
PULSE(0 5 0 1p 1p 1u 2u)

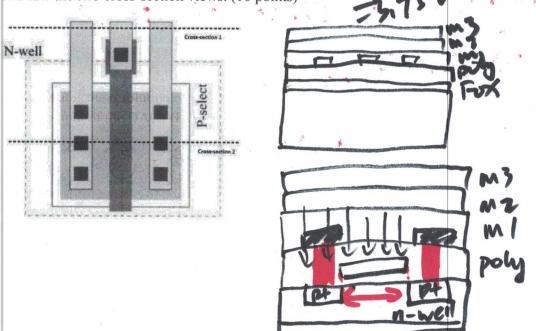
tran 10u

(A) 2MS

$$C_1$$
 C_2
 C_3
 C_4
 C_5
 C_4
 C_5
 C_5
 C_6
 C_7
 C_7

2. (a) What is the resolution of the DAC? (b) What is the digital input of the DAC? (c) What is the analog output of the DAC? (Derivation is not required). (10 points)





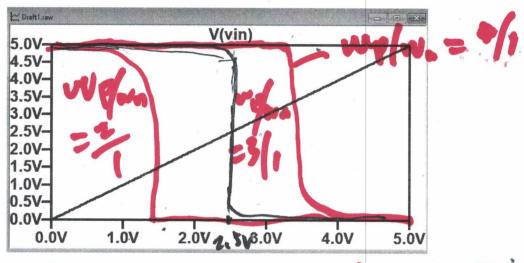
4. Sketch the two I-V curves of NMOS and PMOS respectively (V_{GS} vs I_{DS}, V_{DS} vs I_{DS}, V_{SG} vs ISD, and VSD vs ISD. Label VTHN, VTHP, VDS, sat, VSD, sat, all three operating regions for each type of transistor, (20 points) MAN AOI schematic. (b) Draw the stick diagram of the layout. (10 points) (A + BC)D404BCP 6. Given that the N-Well sheet resistance is 800 ohms/square. (a) What is the resistance of a 300 nm by 1.5 um N-Well wire? (b) What is the resistance of a 500 nm by 2.5 um N-Well wire? (10 points) 160 5

7. An ADC system is required to resolve 1.5 mV analog input. The Reference voltage of the system is 10 V, what is the minimum resolution of the ADC? (10 points)

$$\frac{100}{1.5mV} = \frac{2^{x}}{1.58}$$

$$4 = 105_{2}666667 = 12.07 = 13 \text{ bits}$$

8. Assuming Wp is the width of a PMOS, Wn is the width of an NMOS. The Length of the NMOS and PMOS are the same. Draw Vout1 (Wp/Wn = 2/1) for Inverter 1 and Vout2 (Wp/Wn = 4/1) for Inverter 2 given the following input. It's given that when Wp/Wn=3, the switching point is 2.5 V. (20 points)

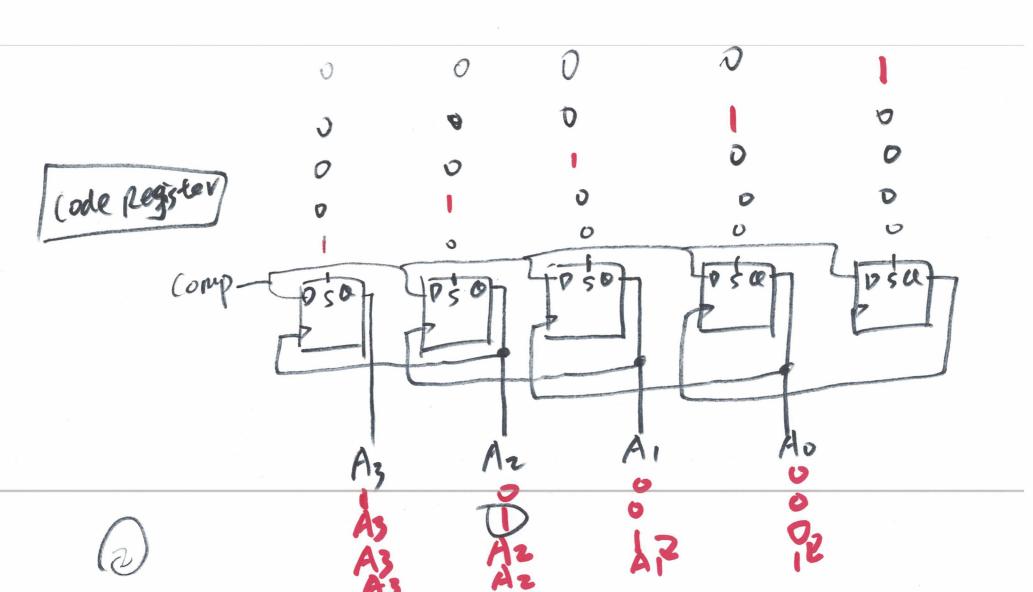


we/whislarger-> stunger Prios

> be able to hold 4t sv

for longer

(AOL= W) SAR Algorithm 7622 Up + Jul Vont = (Up-Vn). ALL 4-bit ADC 6.2V VINTUVAL AS VINE VOAC ASAL



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