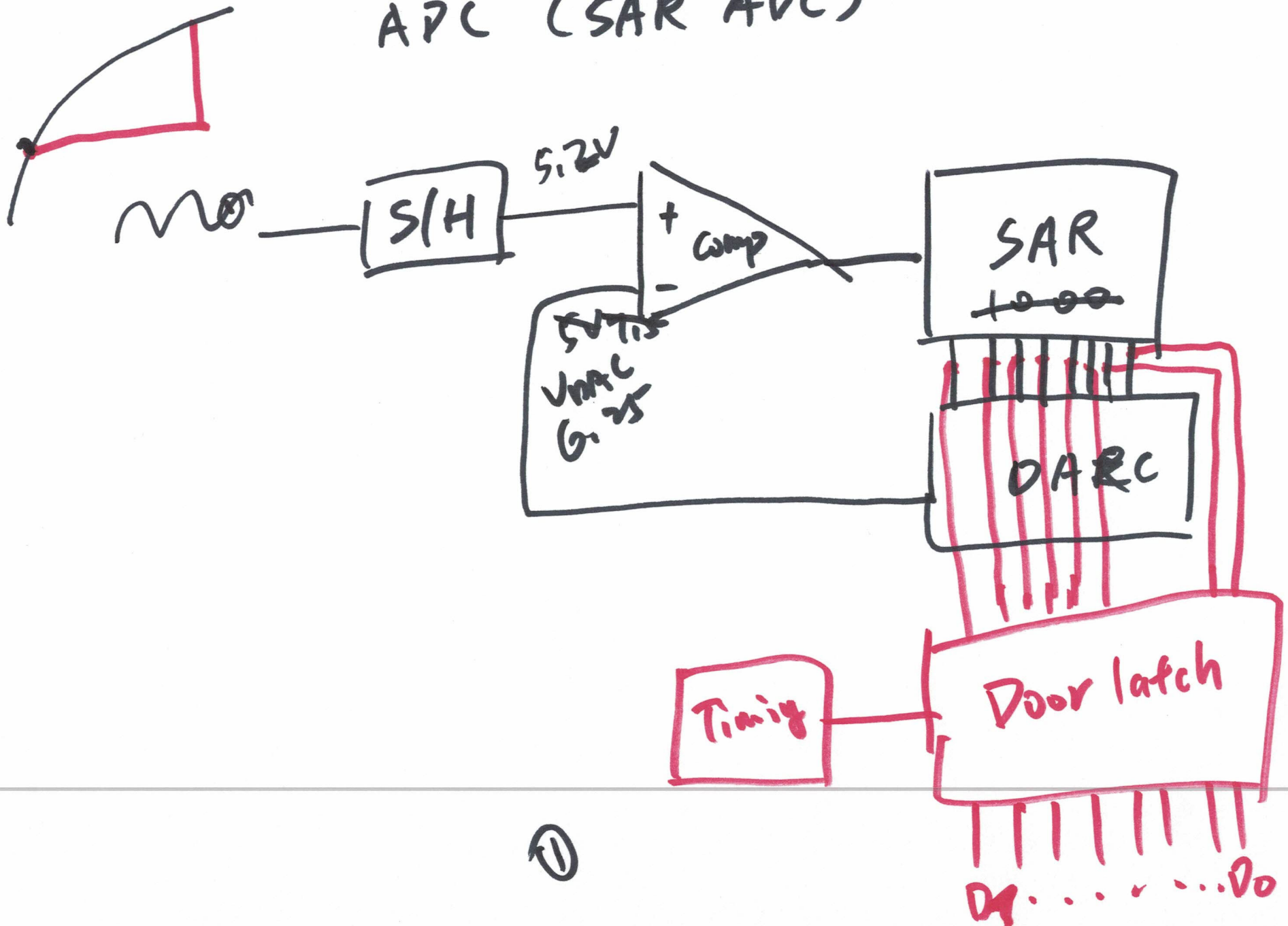
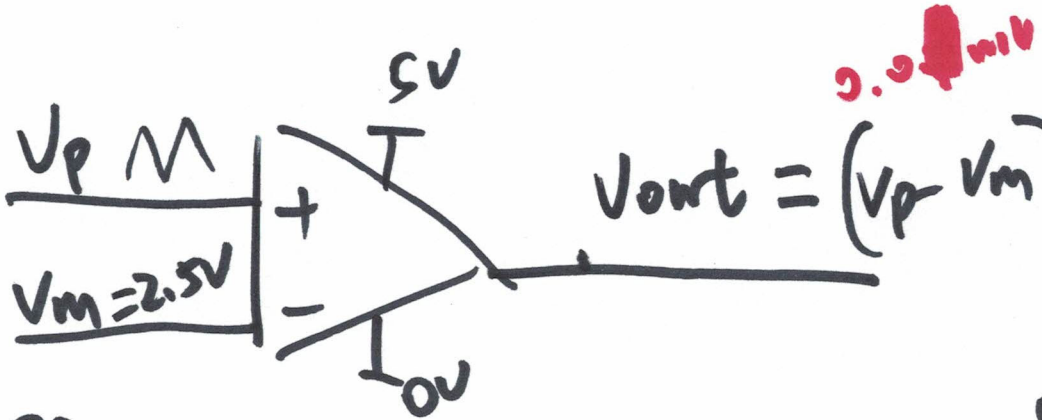
Successive Approximation Register ADC (SAR ADC)

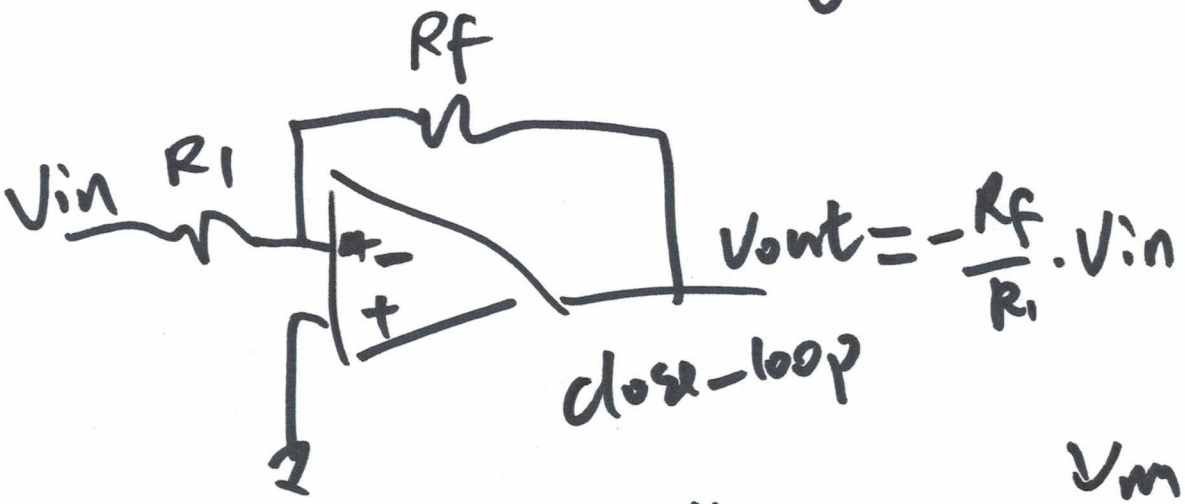




$V_{out} = (V_p - V_m) \cdot A_{OL}$

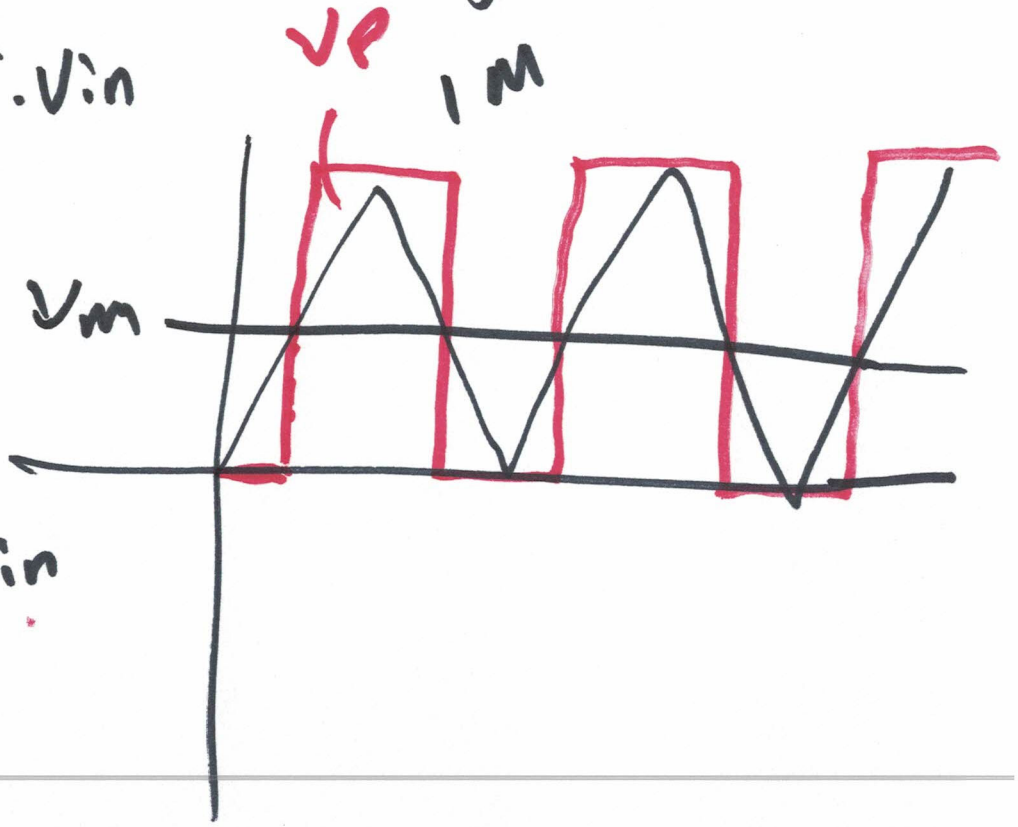
↓

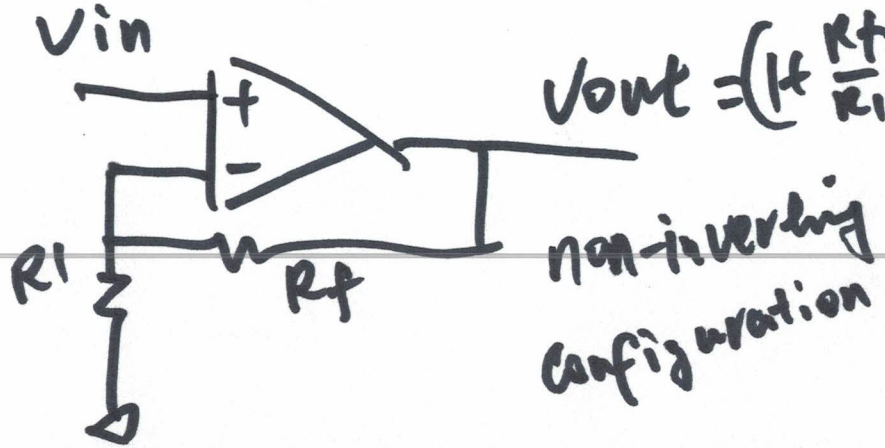
open-loop gain



$V_{out} = -\frac{R_f}{R_1} \cdot V_{in}$

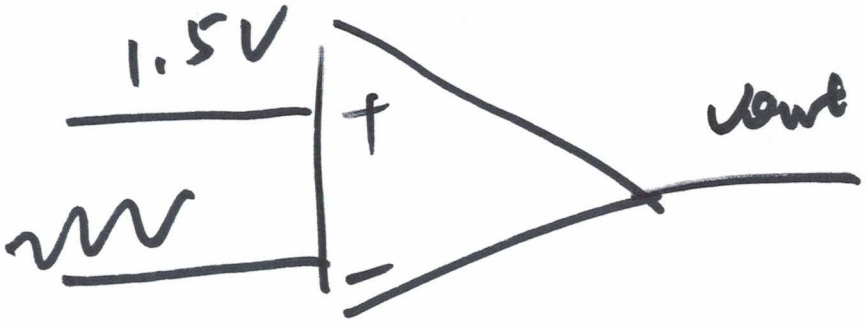
inverting Configuration

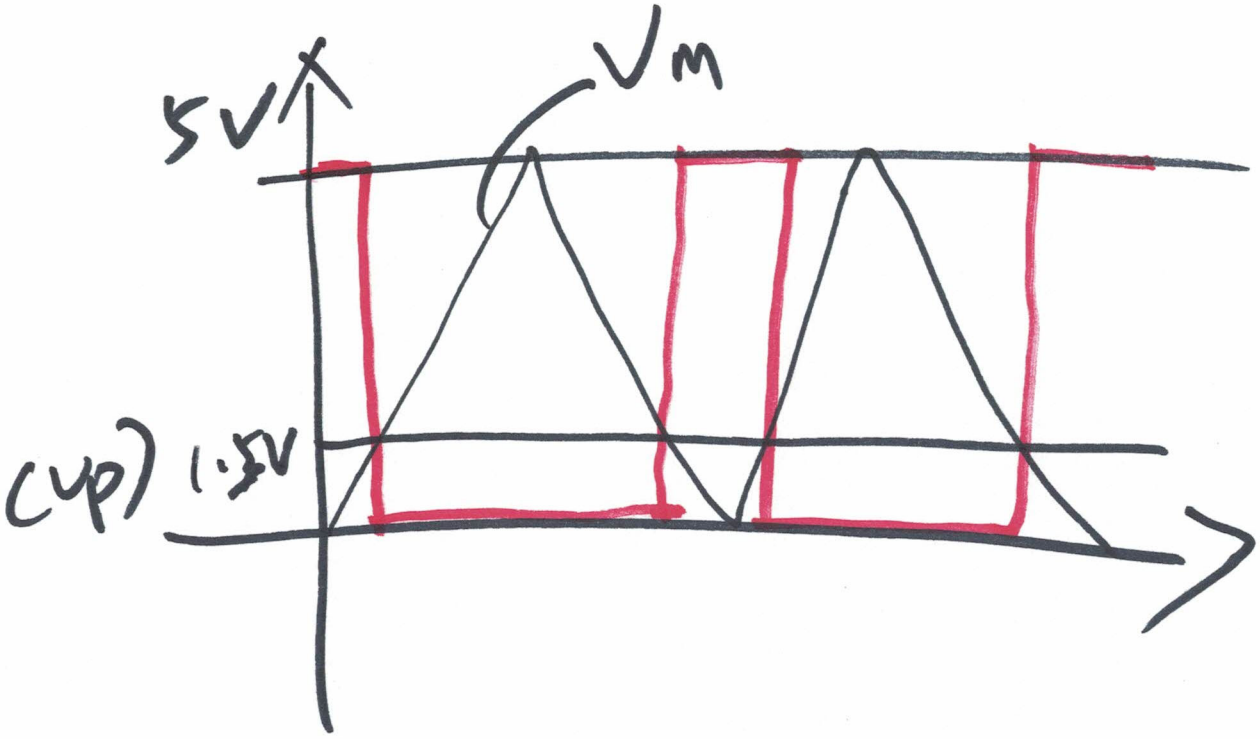


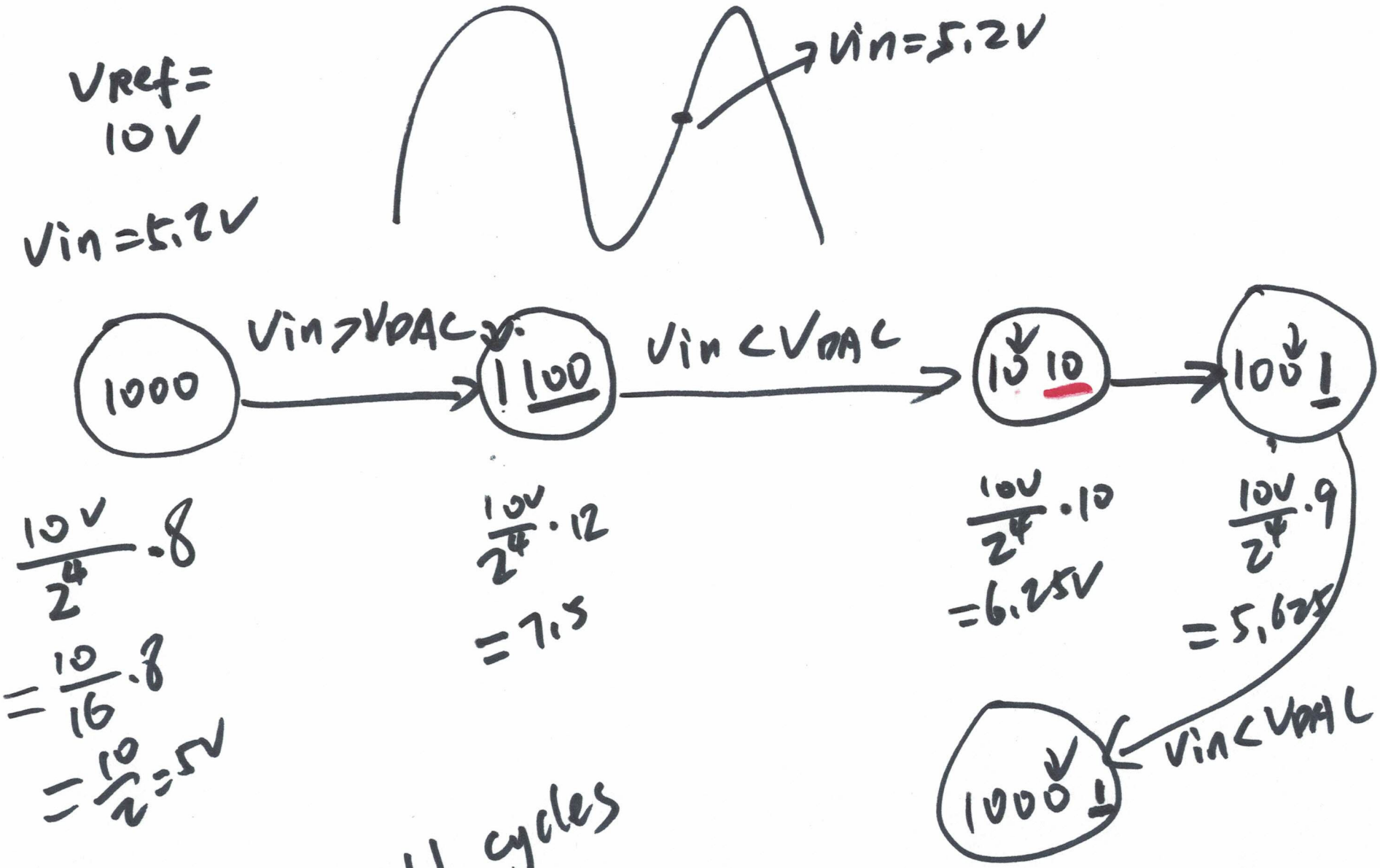


$V_{out} = \left(1 + \frac{R_f}{R_1}\right) V_{in}$

non-inverting configuration

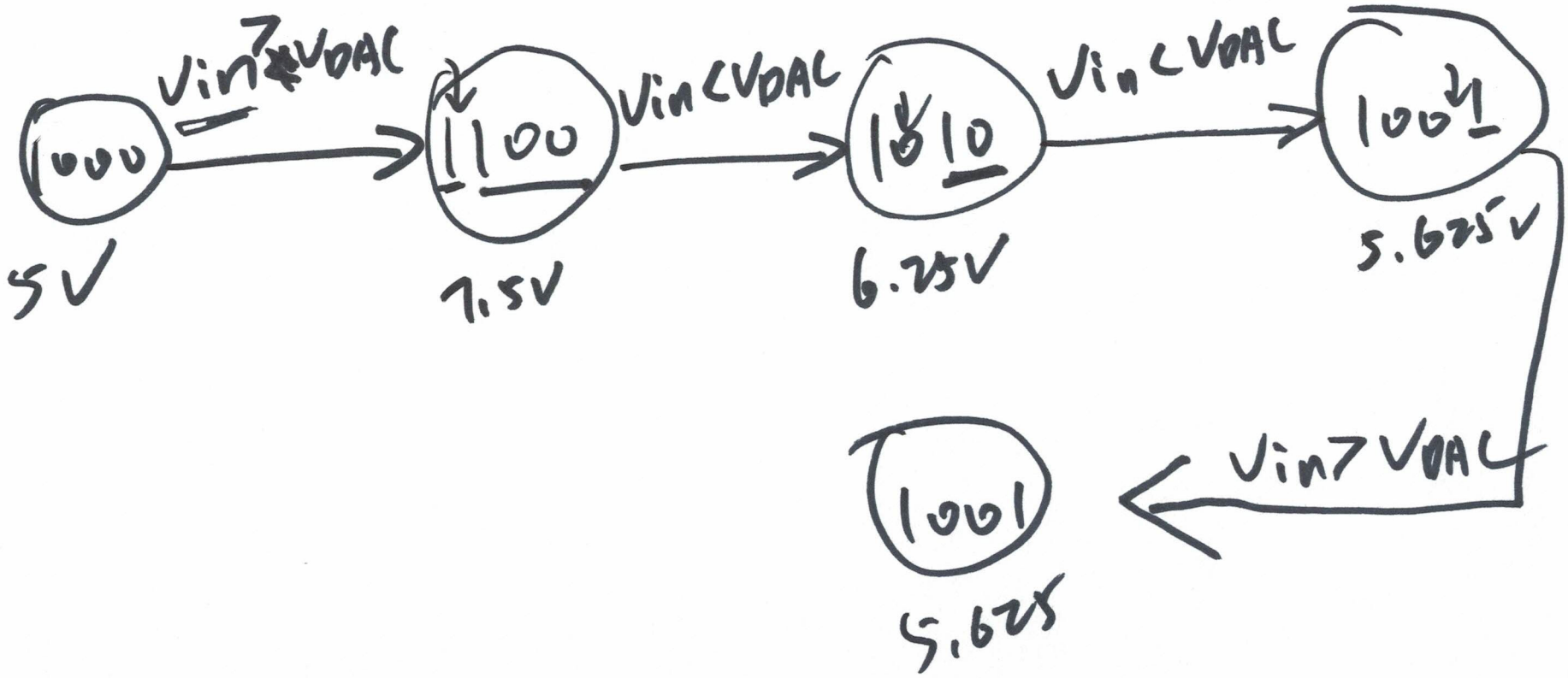

1.5V
+
-
Vout

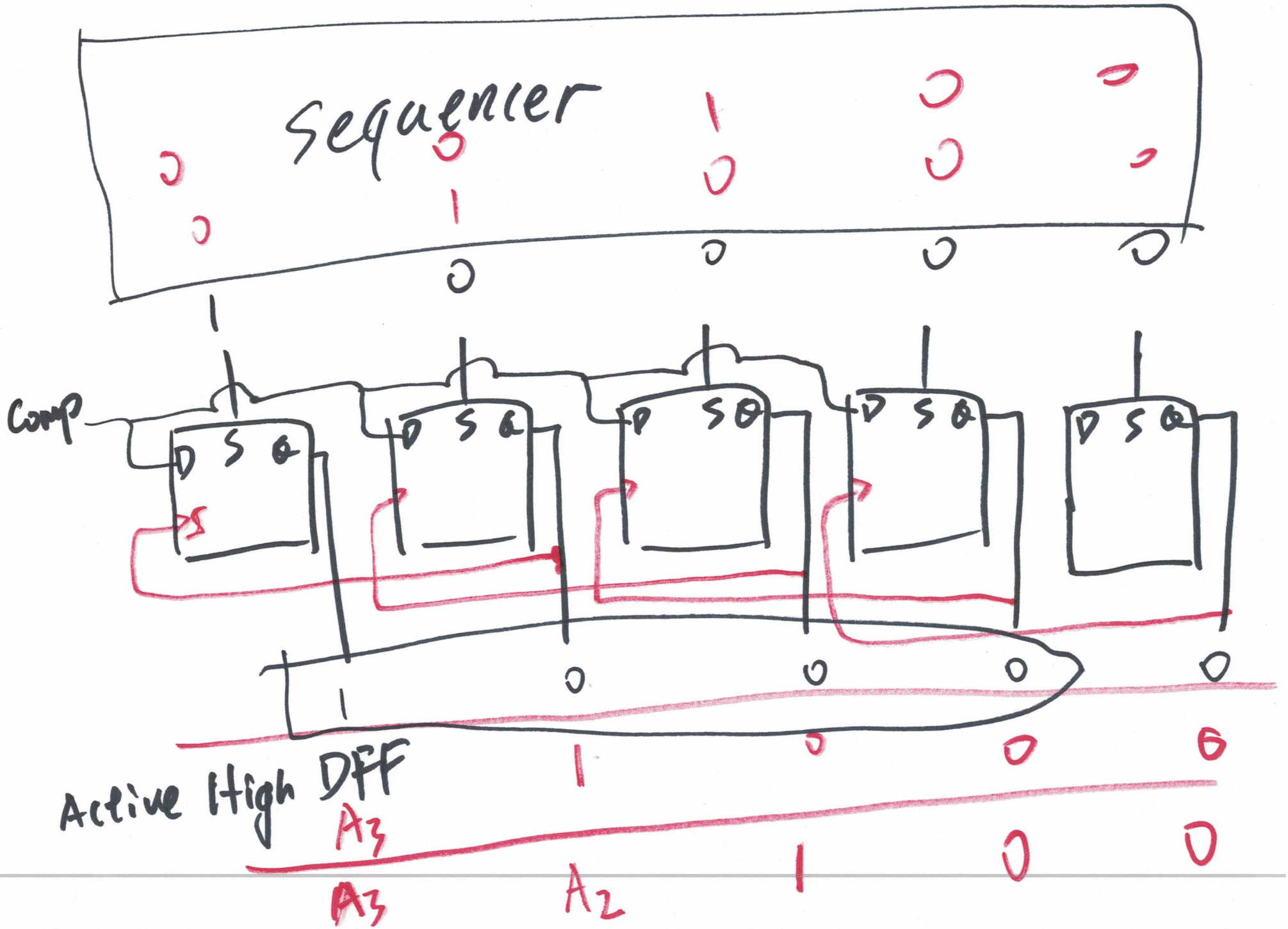

5V
Vm
(vp) 1.5V


VRef=
10V
Vin=5.2V
Vin=5.2V
1000
Vin>VDAC
1100
Vin<VDAC
1310
1001
1000
Vin<VDAC
10V/2^4 .8
=10/16 .8
=10/2=5V
10V/2^4 .12
=7.5
10V/2^4 .10
=6.25V
10V/2^4 .9
=5.625
N+1 cycles
N: resolution
of the ADC
4


6V

$V_{REF} = 10V$


Vin ≥ VDAC
Vin < VDAC
Vin < VDAC
Vin ≥ VDAC
0000
1100
1010
1001
1001
5V
7.5V
6.25V
5.625V
5.625

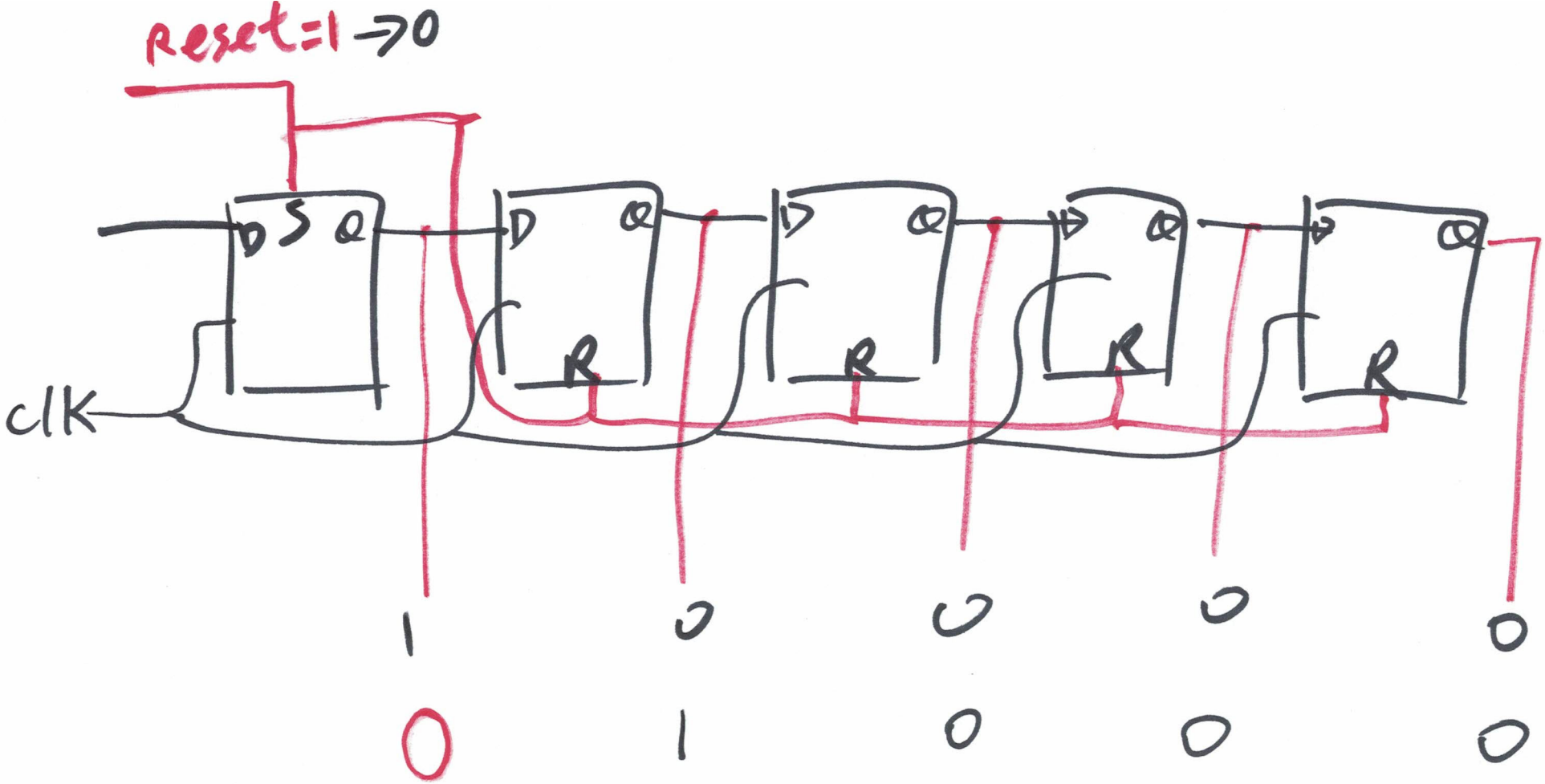


(b)

A_3 A_2 A_1 A_0

cycle #	D_3	D_2	D_1	D_0	Comp Output
0	0	0	0	0	
1	1	0	0	0	A_3
2	A_3	1	0	0	A_2
3	A_3	A_2	1	0	A_1
4	A_3	A_2	A_1	1	A_0
5	A_3	A_2	A_1	A_0	

N+1 cycles


Reset=1 → 0
D
S
Q
R
clk
1
0
0
0
0
0
1
0
0
0