

Fall 2025 Midterm Review

Saturday, February 15, 2025 8:05 PM

quizzes 1-8

HW 1-3

lecture videos / notes

8 problems 55/8 7min 2min

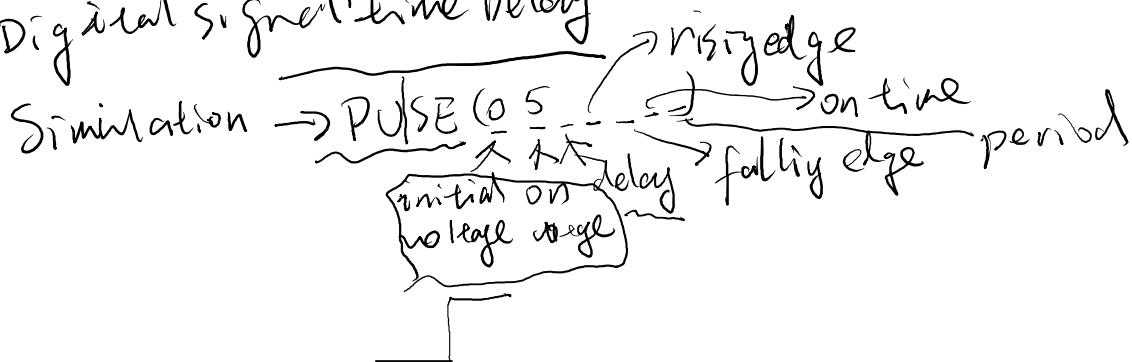
No cheat sheet is allowed

close book close notes

calculator is allowed

Thevenin's equivalent

Digital signal time delay



R-2R DAC

Vout From digital input

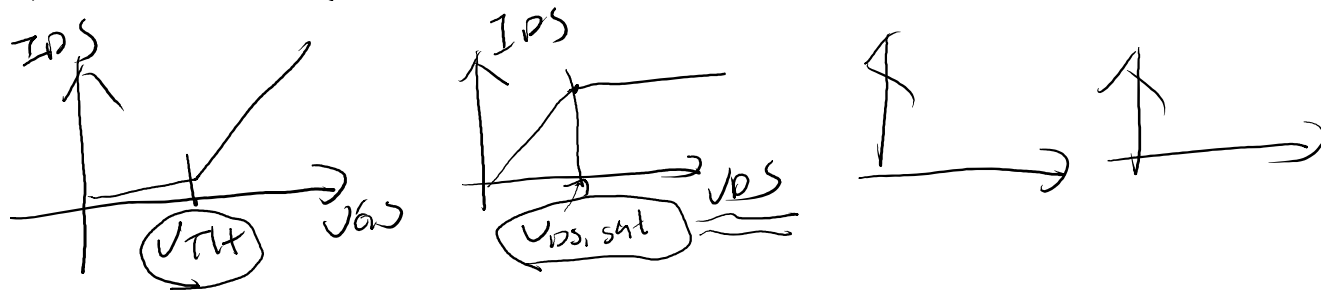
Derivation not required

101 110 Vout

25 layers 3 meter



IV curves of NMOS and PMOS



Diodes, PN Junctions, depletion region

Junction Capacitance. Diode Clamping circuit

AOI logic, schematic, stick diagrams
lecture notes, quizzes, HW

N-well resistors, time delay, sheet resistance
 APC resolution, inverters (notes regarding switching

