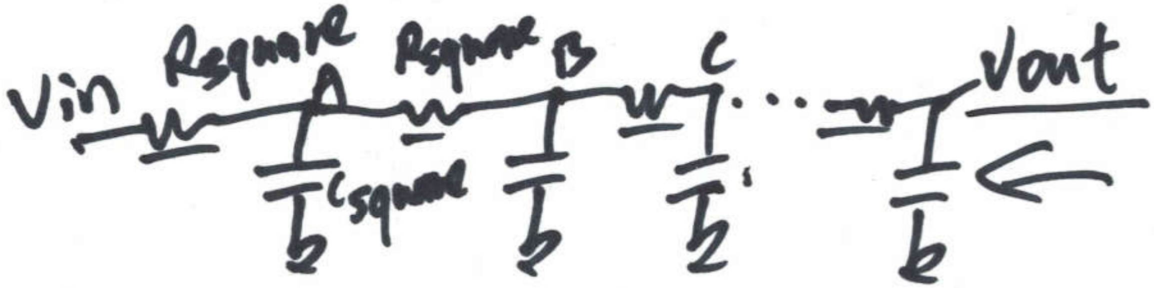
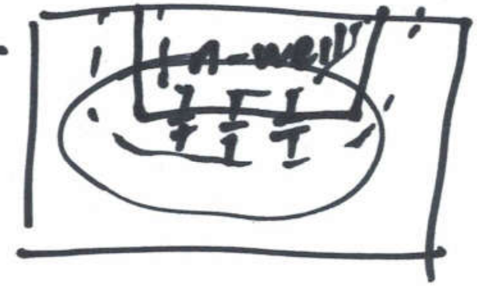
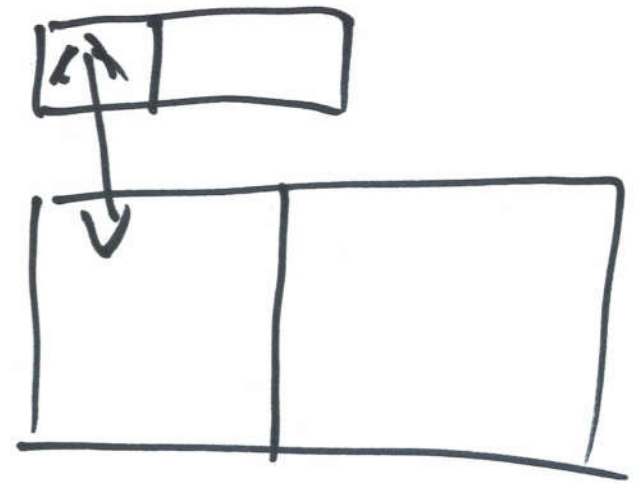
The RC delay through the N-well





$$\begin{cases} t_{dA} = 0.7\, R_{square} C_{square} \\ t_{dB} = 0.7\, 2 R_{square} C_{square} \\ t_{dC} = 0.7\, 3 R_{square} C_{square} \\ \vdots \\ t_{dout} = 0.7 \cdot l \cdot R_{square} C_{square} \end{cases}$$



$$t_d = t_{dA} + t_{dB} + t_{dC} + \cdots + t_{dout} = 0.7\,(1+2+3+\cdots+l)\, R_{square} \cdot C_{square}$$

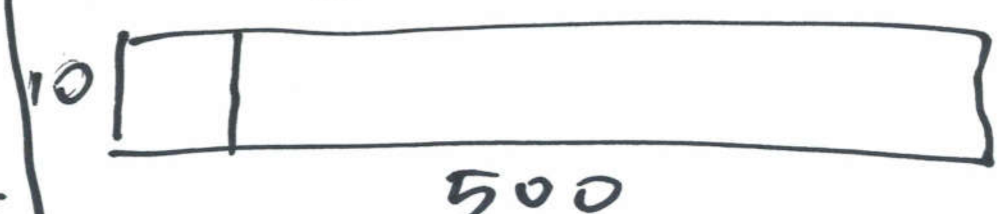
$$= 0.7\, \frac{l(1+l)}{2}\, \underline{R_{square}} \cdot \underline{C_{square}}$$

when l is large.

$$= 0.7 \cdot \frac{l^2}{2} \cdot R_{square} C_{square} = 0.35\, \underline{l^2}\, \underline{R}\, \underline{C}$$

<u>Example:</u> Estimate the time delay through a <u>250kΩ</u> n-well resistor, [redacted] width is 10, length is 500. Assume the capacitance of a 10×10 square of an n-well is <u>5fF</u>.

$$t_d = 0.35 \times 50^2 \cdot \frac{250K}{50} \cdot 5fF$$



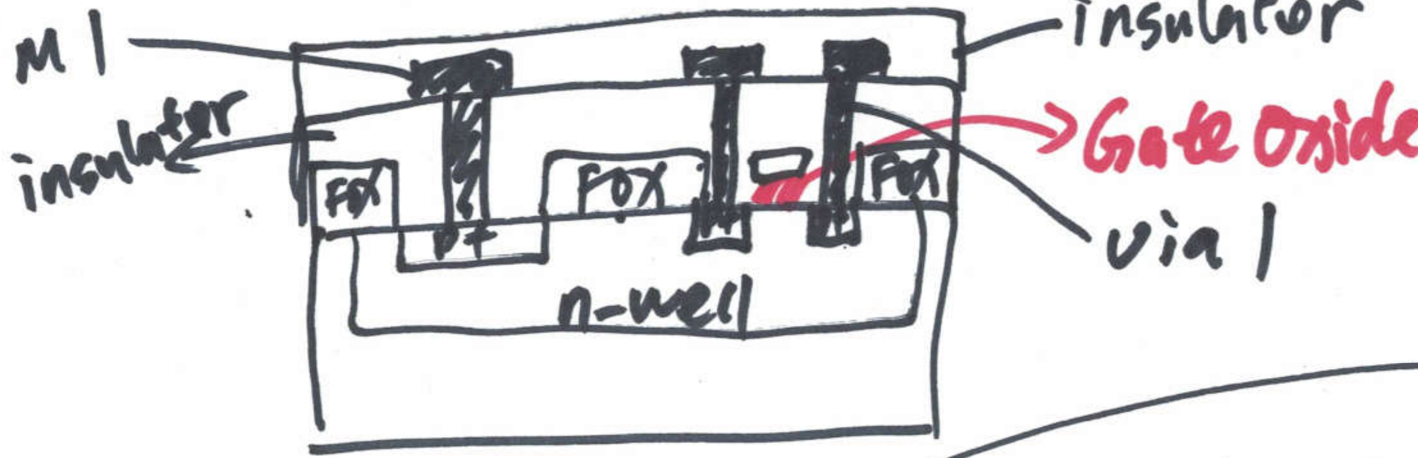
$\frac{500}{10} = 50$ squares

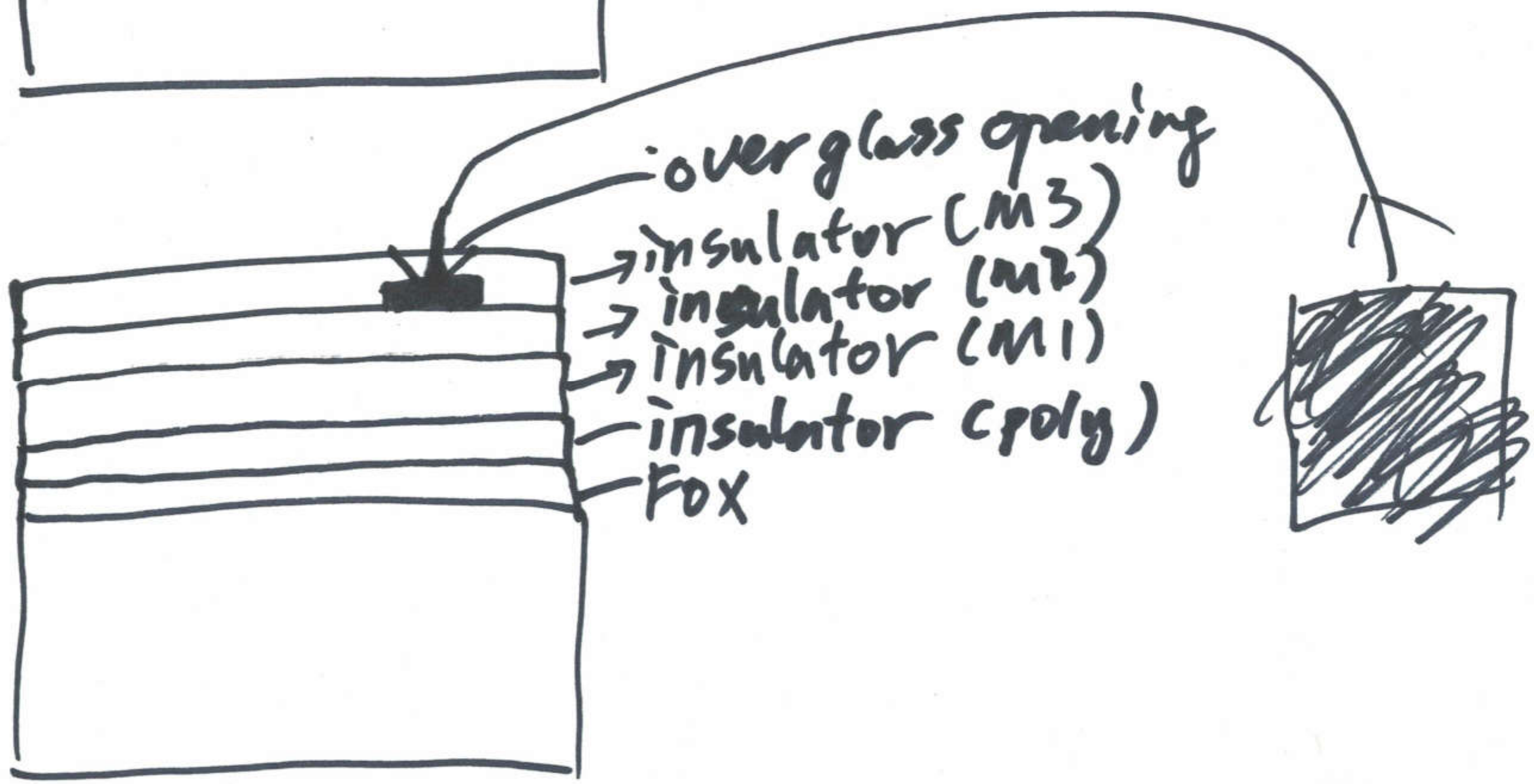
$$= 0.35 \times 2500 \cdot 5K \cdot 5fF$$

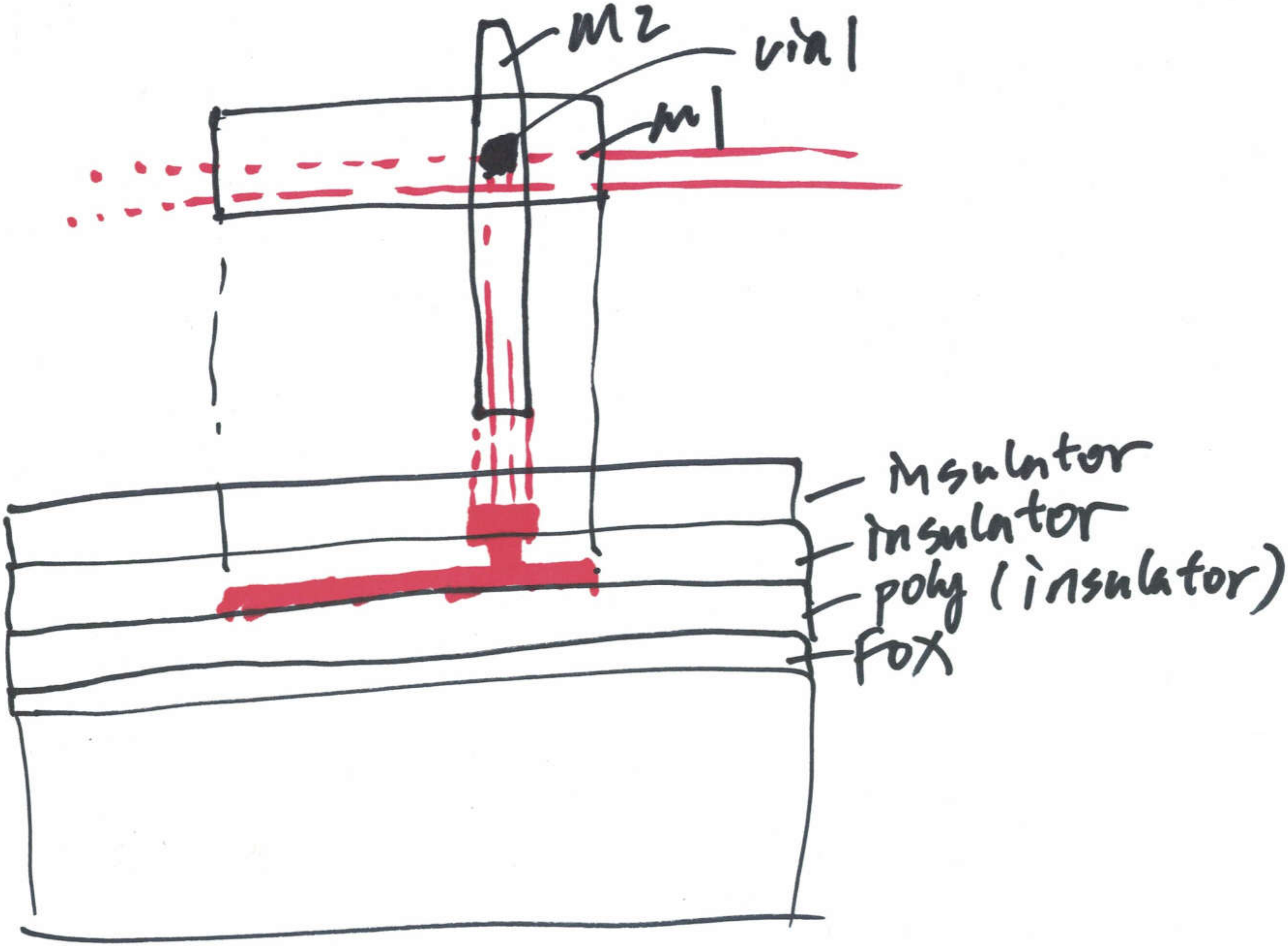
$\rightarrow 10^{-15}$

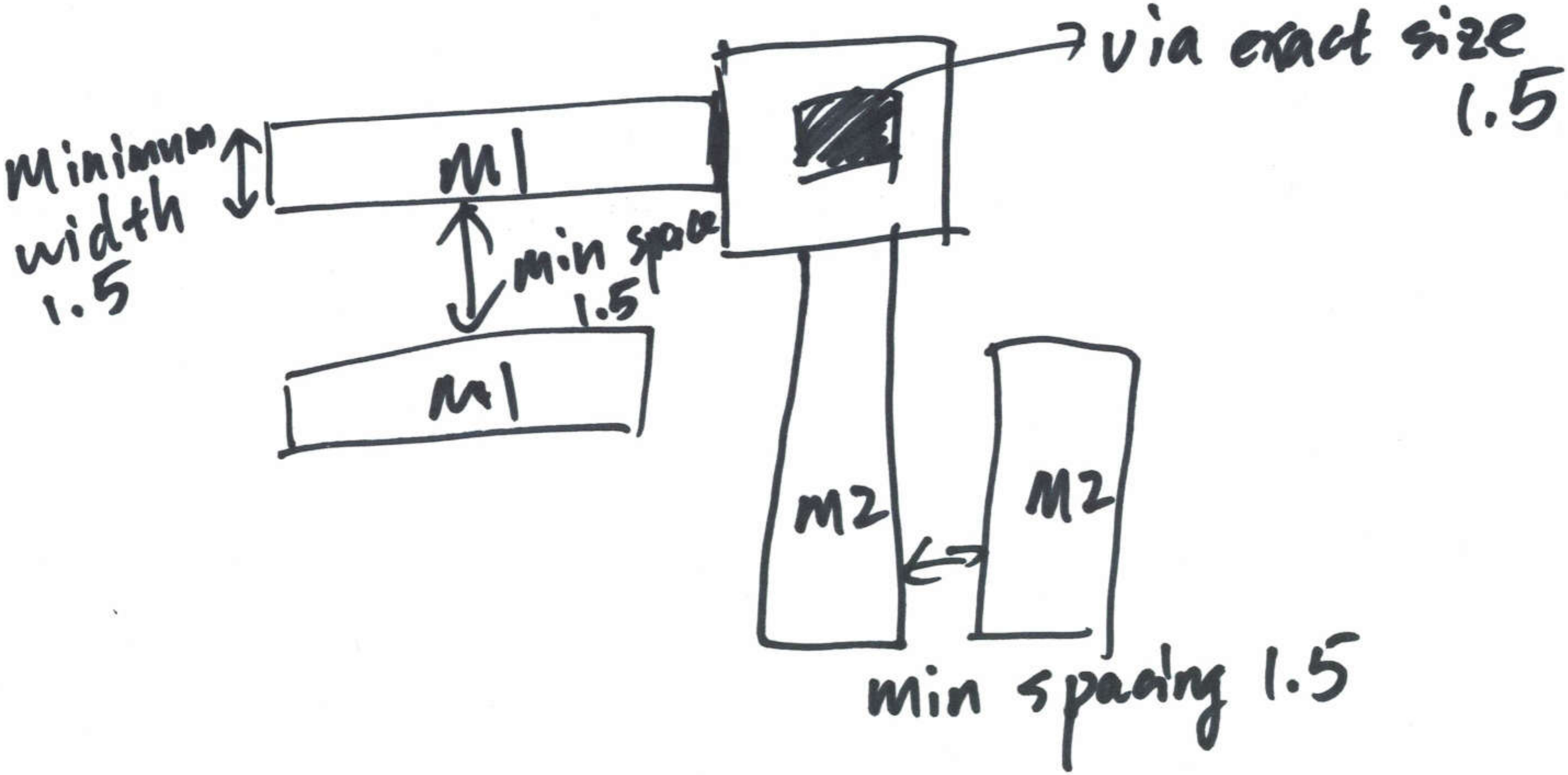
$=$

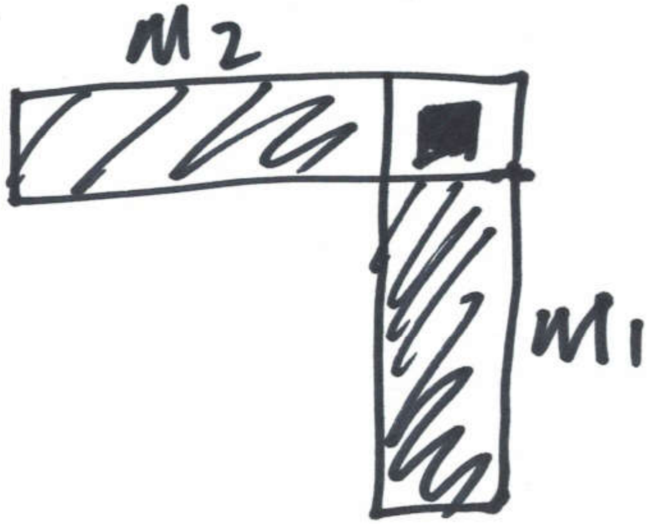
C5 layers

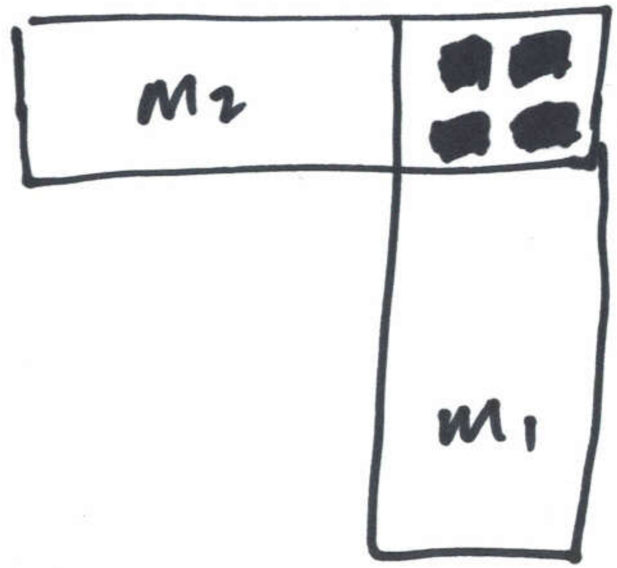

M1
insulator
insulator
FOX
p+
FOX
FOX
n-well
Gate Oxide
via1

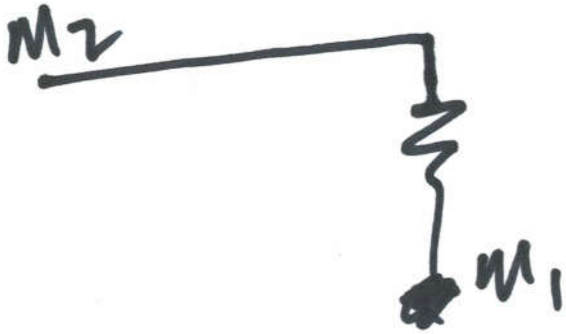

overglass opening
insulator (M3)
insulator (M2)
insulator (M1)
insulator (poly)
FOX

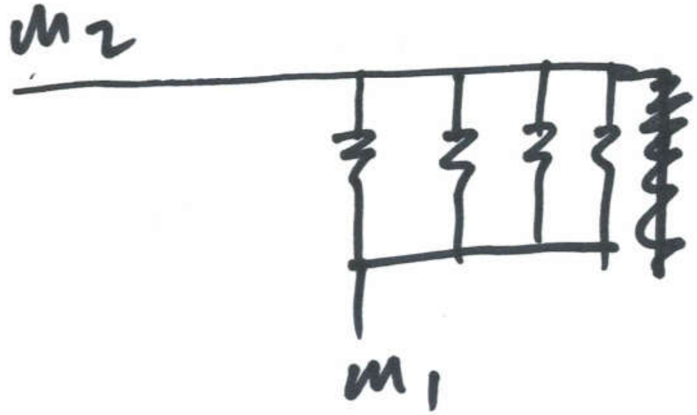

M2
via1
M1
insulator
insulator
poly (insulator)
FOX


via exact size
1.5
Minimum width
1.5
M1
min space
1.5
M1
M2
M2
min spacing 1.5







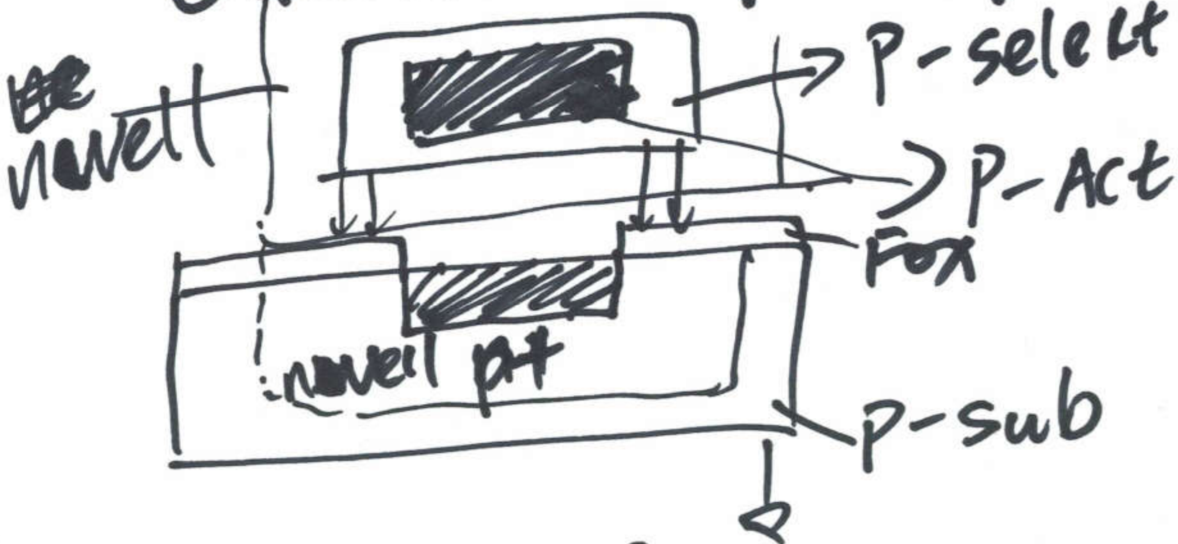


Benefits:

① lower the overall resistance
② lower the current for each via
③ back up vias

The Active and Poly Layers

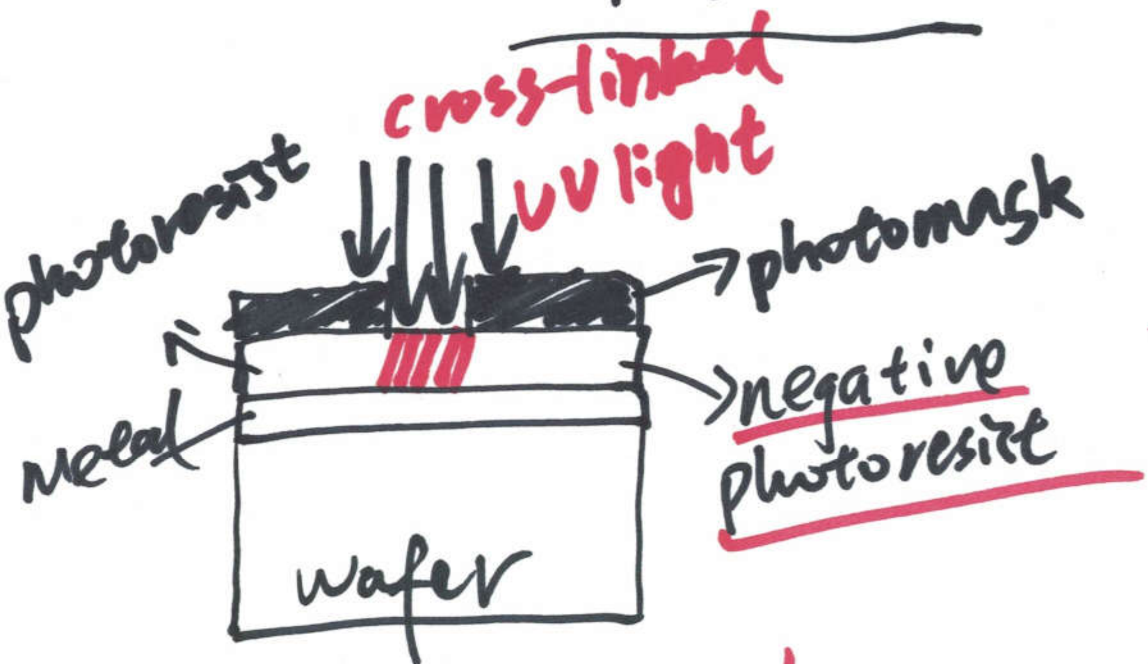
① The Active Layer: opens the Fox



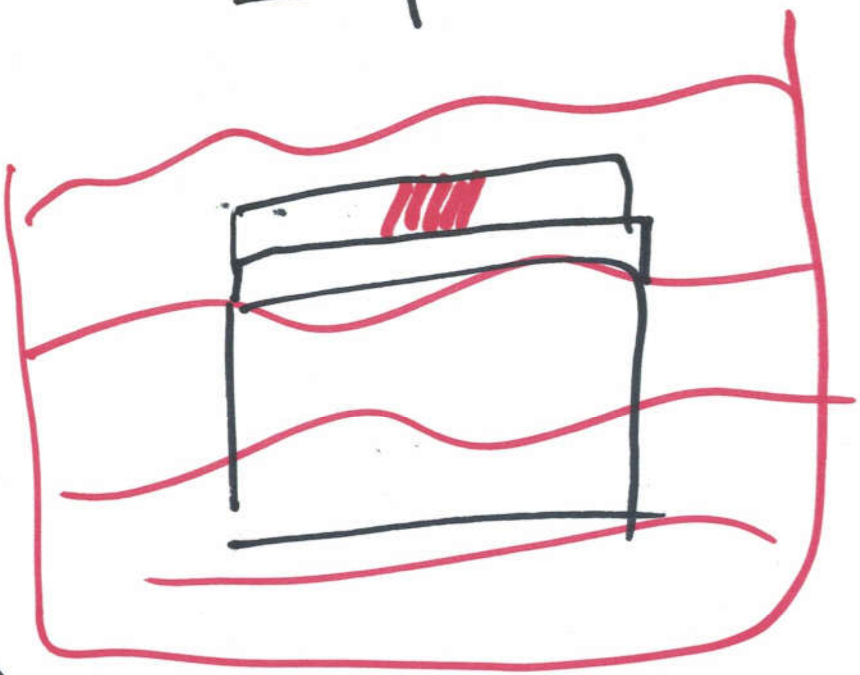
- p-select → p active area
- n-select → n active area

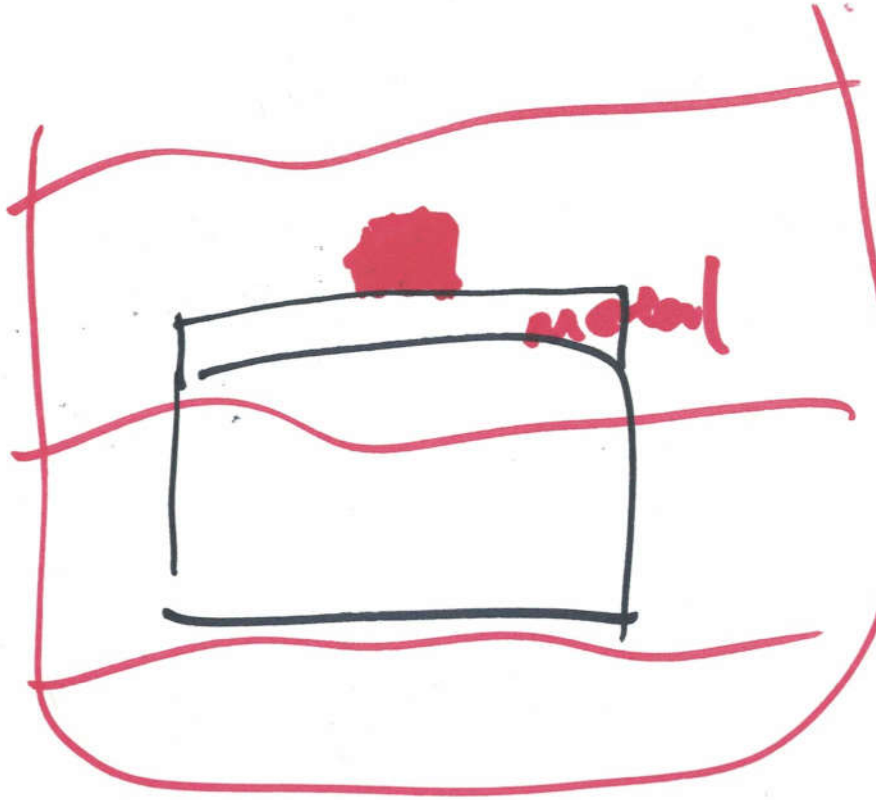
→ minimize the issues of misalignment

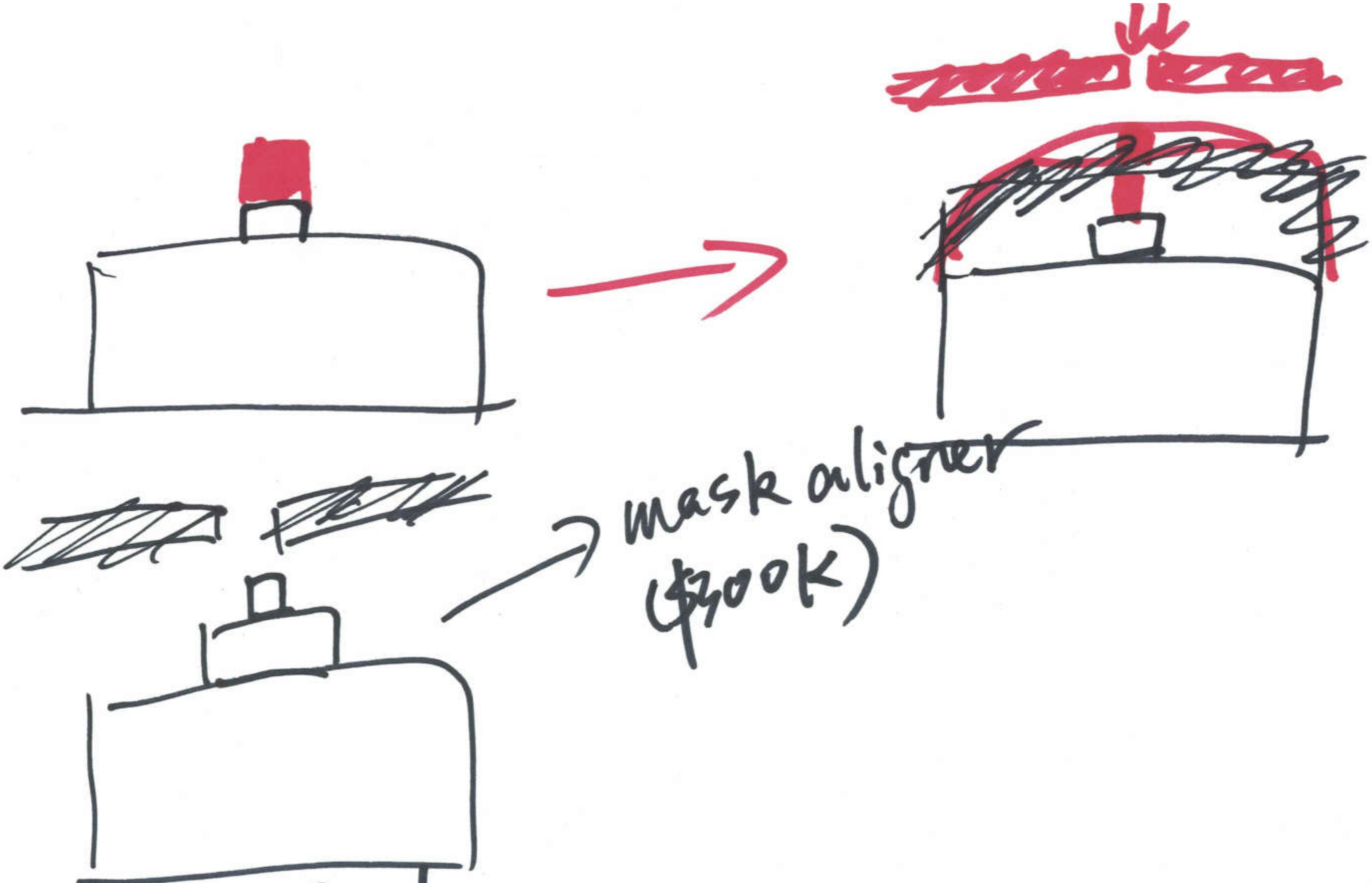
MEMS


cross-linked
UV light
photoresist
photomask
negative photoresist
metal
wafer


wafer




metal



Final Goal