Chapter 2 Semiconductor Basics (pn junction and BJTs)

2.1. Explain what are n_i, n_n, n_p, p_n, p_p, N_A, *and* N_D.

2.2. Consider an n-type silicon for which the dopant concentration N_D=10^17/cm^3. Find the electron and the hole concentration at T=300K (room temperature). Show the calculation process for the credit.

2.3. Find the resistivity of (a) intrinsic silicon and (b) *n*-type silicon with N_D=10^{15}/cm^3. Use n_i=1.5x10^{10}/cm^3, and assume that for intrinsic silicon μ_n=1350 cm^2/V s and μ_p=480 cm^2/V s, and for the doped silicon μ_n=1000 cm^2/V s and μ_p=400 cm^2/V s. (q=1.6x10^{-19} C)

2.4. Draw the pn junction and explain:

1) Without an external voltage, the formation of a depletion region, and the formation of the diffusion current and the drift current.

2) With an external voltage, explain the changes of the width of the depletion region under 'forward bias' and 'reverse bias' operations.

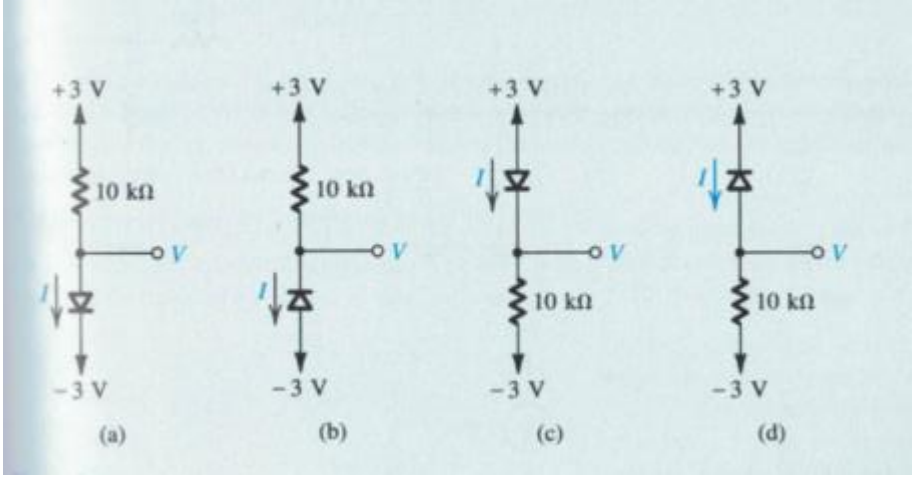
3) Explain how the depletion region will be changed, and how the diode capacitance will be changed with an increasing voltage under both 'forward bias' and 'reverse bias' operations?

4) If a pn junction is reverse biased, is I_D larger or I_s larger? What if it is forward biased?

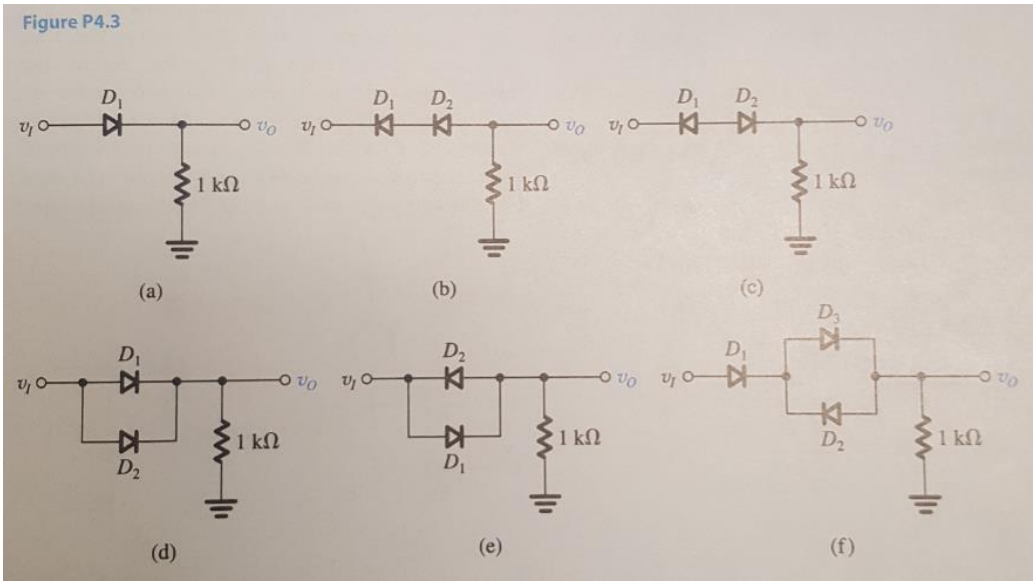
5) Hand-draw the I-V curve of a real diode (with a 0.7 built-in voltage and no reverse breakdown) and the IV curve of an ideal diode.

6) Hand-draw the IV curve of a real Zener diode (with a 0.7 built-in voltage and a -Vz) and the IV curve of an ideal Zener diode.

2.5 Ideal diodes (no built-in voltages and no reverse breakdown) find the values of the voltages and currents indicated in the following figure.

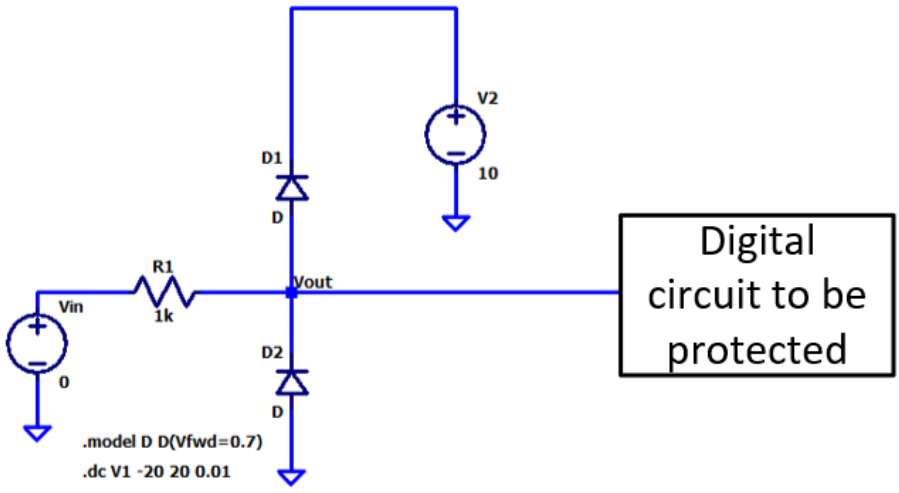


2.6. In the following figure, Vi is a 1kHz 5-V peak-peak sine wave (centered at 0V), sketch the waveform of Vo and label the peak values. (ideal diodes, no built-in voltages and no reverse breakdown)



2.7. The following circuit is being used for ESD (Electrostatic discharge) protection in ICs. The SPICE code is to simulate the accidental high voltage discharge from the input (Vin). Depends on

Vin, draw the Vout of this circuit. (assume 10V is the safe voltage for the digital circuit. You don't need to run this in LTSpice, just hand draw it). (the diodes are real diodes with a 0.7 built-in voltage and no reverse breakdown).

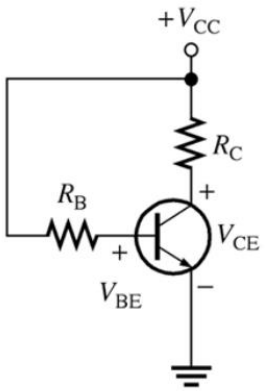


2.8. Consider an npn transistor with V_{BE} = 0.7V at I_C = 1mA. Find V_{BE} at I_C = 10mA (V_T = 25 mV).

2.9. Transistors of a certain type are specified to have β values in the range of 50 to 150. Find the range of their α values.

2.10. Calculate β for two transistors for which α = 0.99 and 0.98. For collector currents of 10 mA, find the base current of each transistor.

2.11 (a) Assume V_{CC} = 8 V, R_B = 300 k and R_C=1 k, β =100. Determine whether the transistor is biased in cutoff, saturation or linear region. (b) Determine the Q-point values of I_C and V_{CE} for the following circuit. (c) Find I_{Cmax} and $V_{CE(cutoff)}$ (V_{CE} when Ic=0A) and hand draw the DC load line and label the Q-point (just simply label the I_C and V_{CE} of the Q point on the load line). (d) Find the maximum peak value of base current for linear operation.



2.12 Select appropriate R_1, R_2, and R_E to bias the following common emitter amplifier in linear region. Given that R_L=2k, V_{CC}=15V, V_{RE}=1V, β =100. (Assume the current flows through R2 is 10 times higher than the Base current).