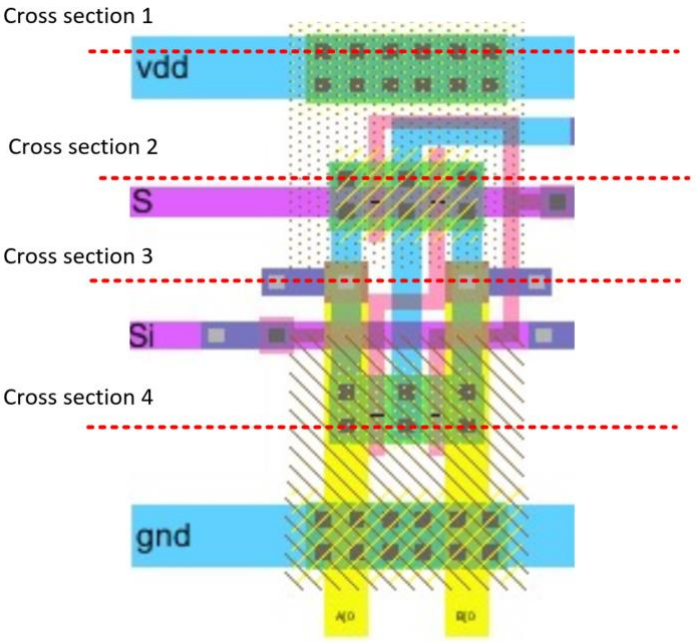
ENGR338 Digital Electronics (120 min, close-book, close-notes, 100 points)

1. Convert the following logic expressions to AOI circuits and **DESIGN** the stick diagram layouts of the following logic circuits. Label the signals at the gates but don't connect the gates with wires (**the stick diagram must NOT be broken in the PMOS and NMOS series – one line for all PMOSes and one line for NMOSes**). (20 points)

a. $\overline{ABCD + CDE + AB}$
b. $\overline{ABC + DE(EF + A)}$

2. Draw the cross-sectional views (indicated by the dashed lines) of the following layout (C5 process). (12 points)



3. **DESIGN** a ring oscillator using the 1um technology and the standard CMOS transistors in the following table so the oscillation frequency will be somewhere around 500 MHz (and no slower than 500 MHz). Show the calculation and draw the resistive/capacitive digital model of the circuit (only need to include two inverters in the model). (18 points)

Table 10.2 Parameters for general digital design using the long-channel (scale factor is 1 μm) or short-channel (scale factor of 50 nm) CMOS process **used in this book**.

Technology	Drawn	Actual size	$R_{n,p}$	$C_{ox,n,p}$
NMOS (long-channel)	10/1	10 μm by 1 μm	1.5k	17.5 *fF*
PMOS (long-channel)	30/1	30 μm by 1 μm	1.5k	52.5 *fF*
NMOS (short-channel)	10/1	0.5 μm by 50 nm	3.4k	625 *aF*
PMOS (short-channel)	20/1	1 μm by 50 nm	3.4k	1.25 *fF*

4. Estimate the time delay from D to A and D to B (including t_{PHL} and t_{PLH}). Show the parasitic capacitors in the schematic. Use the 50 nm CMOS transistors in the following table. (14 points)

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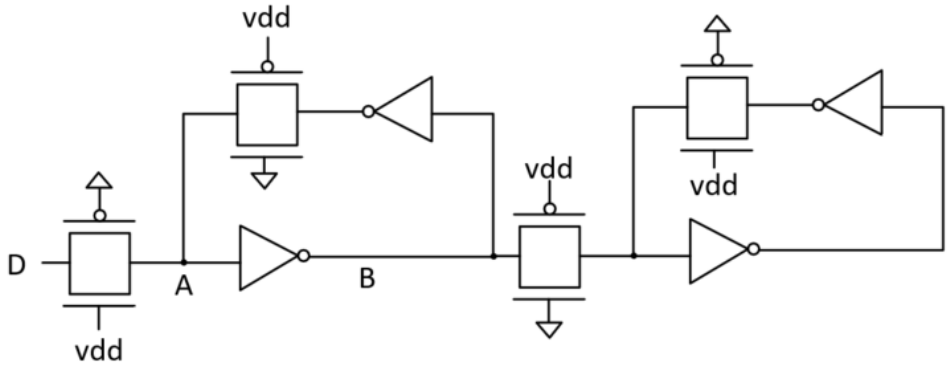
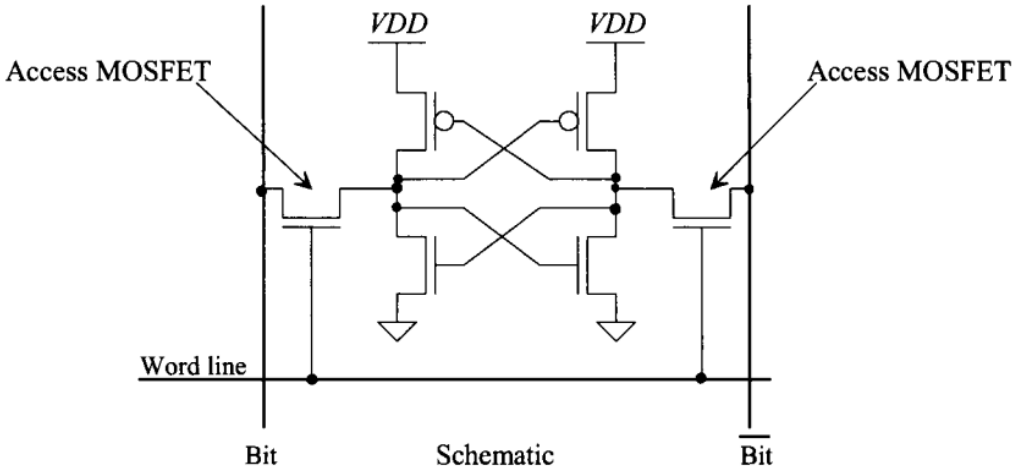


5. (a) What do SRAM, DRAM, and SDRAM stand for? (b) Name 2 fabless, 2 IDM, and 2 pure play foundries in the current semiconductor industry. (c) What is Moore's Law? (d) When were the following process nodes commercialized:180 nm, 65 nm, 22 nm, 10 nm, and 5 nm? (16 points)

6. What is the following memory cell? Describe the Read and Write operations. (Add necessary parts/circuits to it to help your interpretation). (10 points)



7. Assume V_{CC} = 8 V, R_B = 300 k and R_C=1 k, β =100. Determine whether the transistor is biased in cutoff, saturation or linear region. (b) Determine the Q-point values of I_C and V_{CE} for the following circuit. (c) Find I_{Cmax} and $V_{CE(cutoff)}$ (V_{CE} when Ic=0A) and hand draw the DC load line and label the Q-point (just simply label the I_C and V_{CE} of the Q point on the load line). (d) Find the maximum peak value of base current for linear operation. (10 points)