Fort Lewis College

COURSE SYLLABUS

CE 338: Digital VLSI Design

4 Credits

*(Lectures/Labs)*

***Land Acknowledgement:*** *"We acknowledge the land that Fort Lewis College is situated upon is the ancestral land and territory of the Nuuchiu (Ute) people who were forcibly removed by the United States Government. We also acknowledge that this land is connected to the communal and ceremonial spaces of the Jicarilla Abache (Apache), Pueblos of New Mexico, Hopi Sinom (Hopi), and Diné (Navajo) Nations. It is important to acknowledge this setting because the narratives of the lands in this region have long been told from dominant perspectives, without full recognition of the original land stewards who continue to inhabit and connect with this land. Thank you for your attention and respect in acknowledging this important legacy."*

**Instructor:** Dr. Yiyan Li
**Lectures:** MWF: 12:20 – 1:15 pm, BH570
**Labs on Tuesdays:** 11:15 am – 2:20 pm, BH570
**Office Hours: Tuesday 9-11 am and 2:30-3:30 pm; Wednesday & Friday 1:30-3:00 pm.**

## Course Description

This course focuses on transistor-level design of digital blocks for Very Large Scale Integrated Circuits (VLSI), with an emphasis on CMOS technology. Students will learn to design digital blocks and basic circuit components using the three-metal-layer CMOS structure, employing manual techniques such as AOI logic, stick diagrams, and simple circuits like a SAR ADC. The course covers both open-source tools (ElectricVLSI, LTSpice) and industry-standard platforms (Cadence Design Systems) for VLSI layout and simulation. In the final labs, students will gain hands-on experience with modern VLSI design flows using the TSMC 180nm technology, Cadence Genus for synthesis, and Innovus for place-and-route, preparing them for front-end and back-end VLSI design roles in the industry.

## Course Materials & Resource

*CMOS Circuit Design, Layout, and Simulation, Third Edition, R. Jacob, Baker. (required)*

*CMOS VLSI Design: A Circuits and Systems Perspective 4th Edition, Neil Weste, David Harris. (Optional).*

## Course Topics

Review of circuit analysis theories

- Semiconductor Basics
- ADC/DAC Basics
- The N Well
- C5 Layers
- Active and Ploy Layers
- Models for Digital Design
- Static Logic Gates
- Bipolar Junction Transistors
- MOSFETs
- The Semiconductor Industry, Yield, and Defects
- Memory Circuit Design

**Grading Policies**

70% Homework/Quizzes/Lab Reports

10% Midterm

10% Project

10% Final

**Grading Scale by %:**

| Letter Grade | Point Range |
|---|---|
| A | 93-100 |
| A- | 90-92 |
| B+ | 87-89 |
| B | 83-86 |
| B- | 80-82 |
| C+ | 77-79 |
| C | 73-76 |
| C- | 70-72 |
| D+ | 67-69 |
| D | 63-66 |
| D- | 60-62 |
| F | 0-59 |

## Course Outcomes

After completing CE 338 students will be able to:

List the main layers used in the fabrication of a digital integrated circuit. (1, 6)

Sketch the cross-sectional view of a layout. (6)

Design combinational and sequential logic circuits. (1, 2, 6)

Discuss the movement of electrons and holes in pn-junctions and transistors under various operating conditions. (1)

Calculate delays through semiconductor materials and conducting wires. (1)

Layout digital circuits and chips. (1, 6)

## Engineering Program Student Learning Outcomes (ABET criteria)

1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.
2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural social, environmental, and economic factors.
3. an ability to communicate effectively with a range of audiences.
4. an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.
5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgement to draw conclusions.
7. an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

## Course Policies

### Attendance

Attendance is defined to be: in class on time, in class for the duration of the class period, prepared for the day's topic, participation in class.

### Disenrollment Policy

You will be disenrolled from this course if you miss the first day of class and the first laboratory session. If you are disenrolled from the class, you may re-register if space is available.

**Course Withdrawal Information**

Withdrawal from Course – See Registrar's Office website. The date is a college-wide deadline that is not negotiable.

To withdraw from this course, go to the Registrar's Office, Room 160, Miller Student Services Building before the course withdrawal deadline. They will help you through the process. You do not need my signature on the course withdrawal request form.

Starting Fall 2013, students have a lifetime limit of three individual course withdrawals from FLC courses. If you have withdrawn from classes before Fall 2013, these will not count towards your lifetime limit. Also, withdrawing entirely from a semester (all classes) does not count against your lifetime "CW" limit. Semester withdrawal is handled under a different policy and procedure. Please refer to the Academic Policies section of the Fort Lewis College Catalog of Courses for more information about the course and semester withdrawal policies and procedures.

**Canvas**

Online materials (lecture notes, homework assignments, quizzes) will be available at Canvas or on the professor's course webpage. If you are not familiar with Canvas, please work through the Student Canvas Orientation. For technical help with Canvas contact the 24/7 support hotline at 855-971-1611 or submit a HELP ticket in Canvas.

**Course Expectations**

Credit Hour Syllabus Statement

In addition to spending 3 hours per week attending class, the typical student in this 4 credit lecture course/labs should expect to spend at least 6 hours per week of concentrated attention on course-related work, including but not limited to time spent reading, reviewing, organizing notes, preparing for upcoming quizzes/ exams, problem solving, developing and completing projects, and other activities that enhance learning.

**Academic Integrity**

Academic dishonesty includes all forms of unethical or illegal behavior which affects a student's academic standing, including, but not limited to, cheating on exams, plagiarism, forgery of academic documents, falsification of information on academic documents, or unauthorized access to computer files containing academic information. Academic dishonesty may result in sanctions ranging from a lowered grade on a particular assignment to an "F" in the class and report submitted to the Office of the Vice President of Academic Affairs.

****"Fort Lewis College is committed to providing all students a liberal arts education through a personalized learning environment. If you think you have or you do have a documented disability which will need reasonable academic accommodations, and/or if you are a Veteran who may need services, please contact the Disability Services Office, 280 Noble Hall, 970-247-7383, disabilityservices@fortlewis.edu for an appointment as soon as possible."