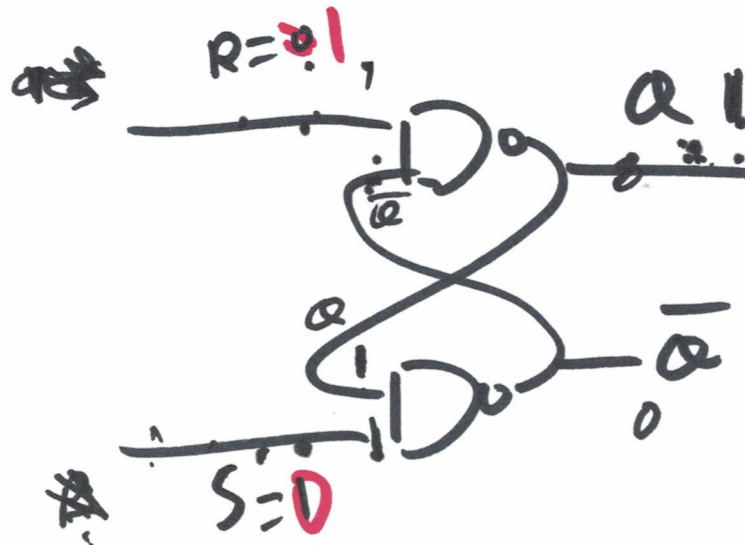
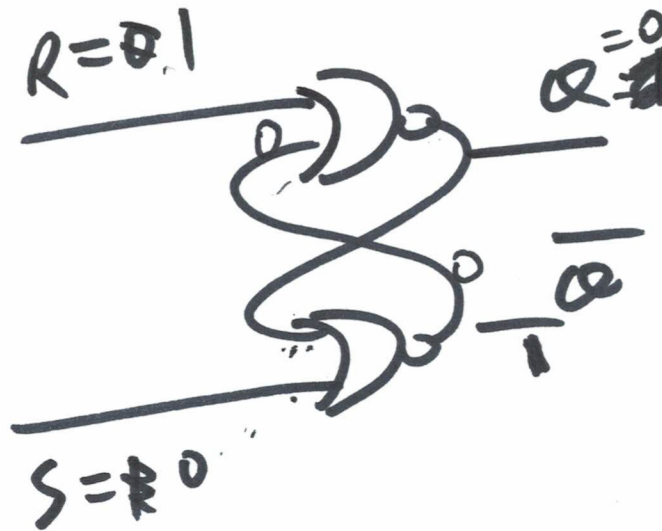


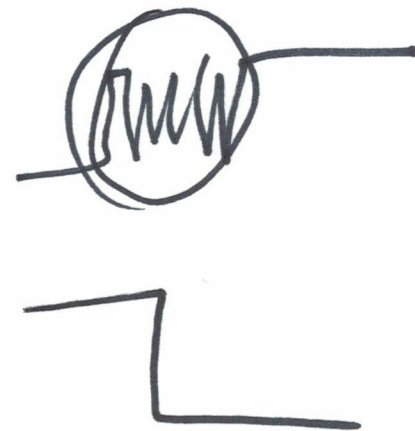
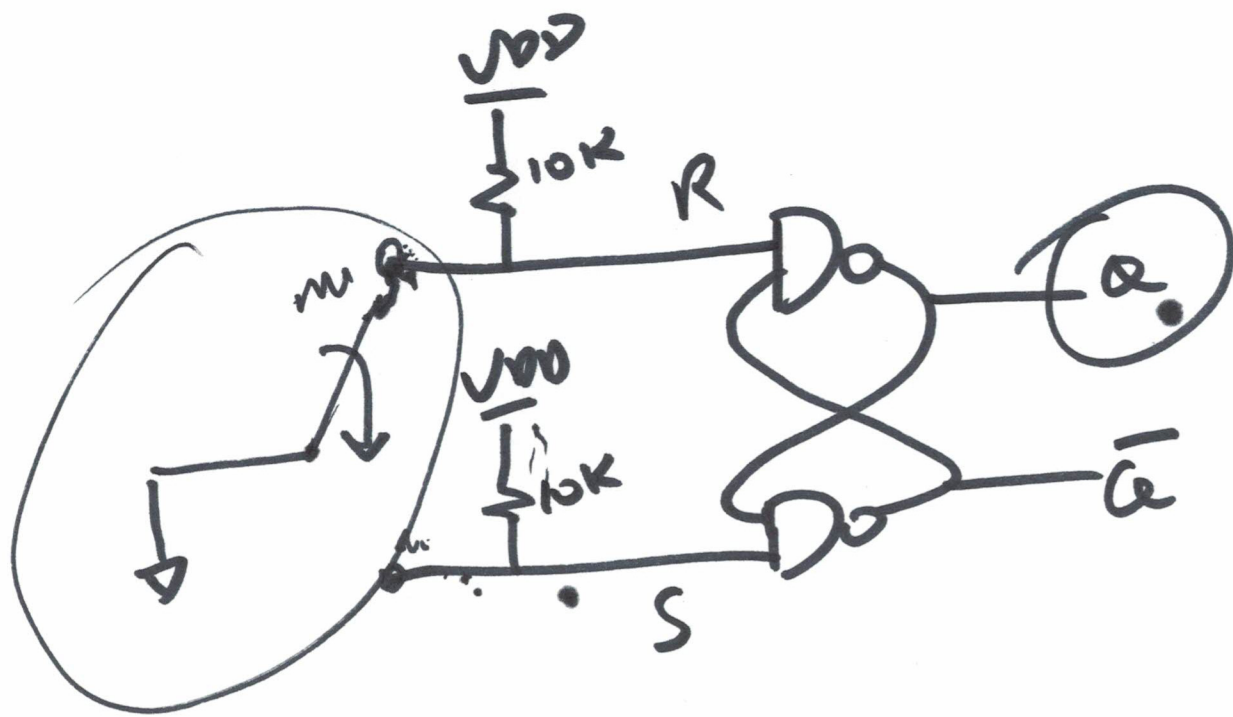
NAND SR Latch set reset



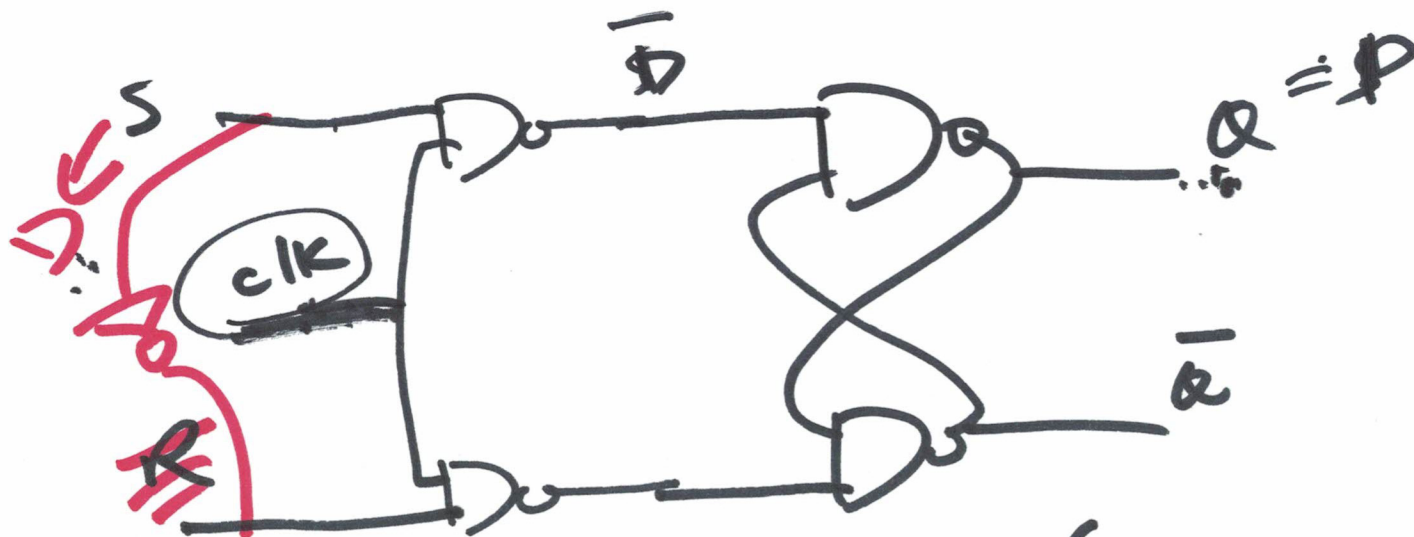
S	R	Q	Q-bar
1	0	1	0
0	1	0	1
1	1	Memory	
0	0	Not used	



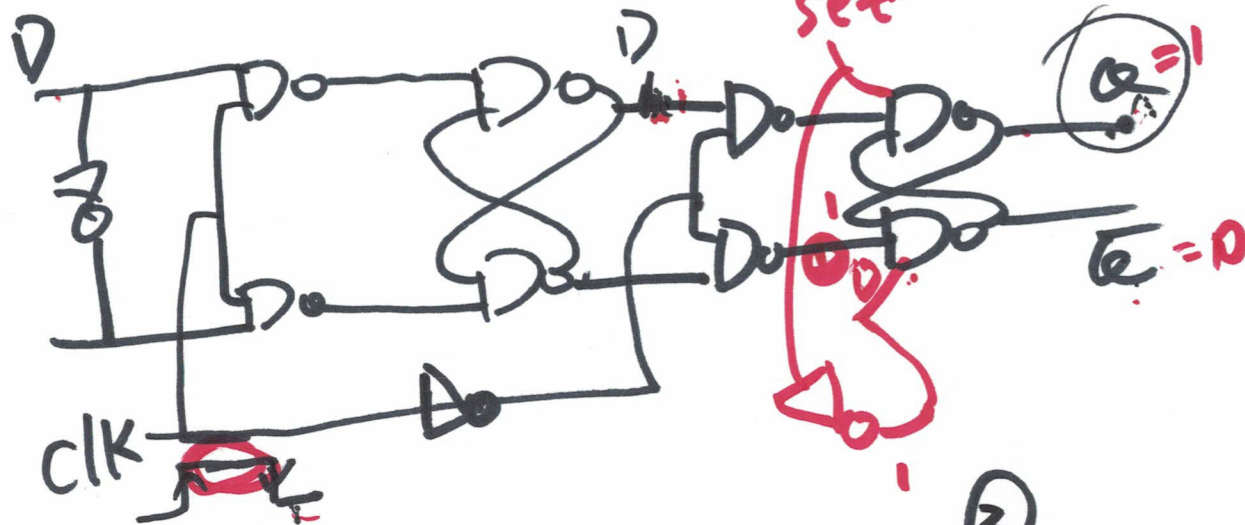
S	R	Q	Q-bar
0	1	0	1
1	0	1	0
1	1	Not used	
0	0	memory	



②



SR flip flop / SRFF
level triggered

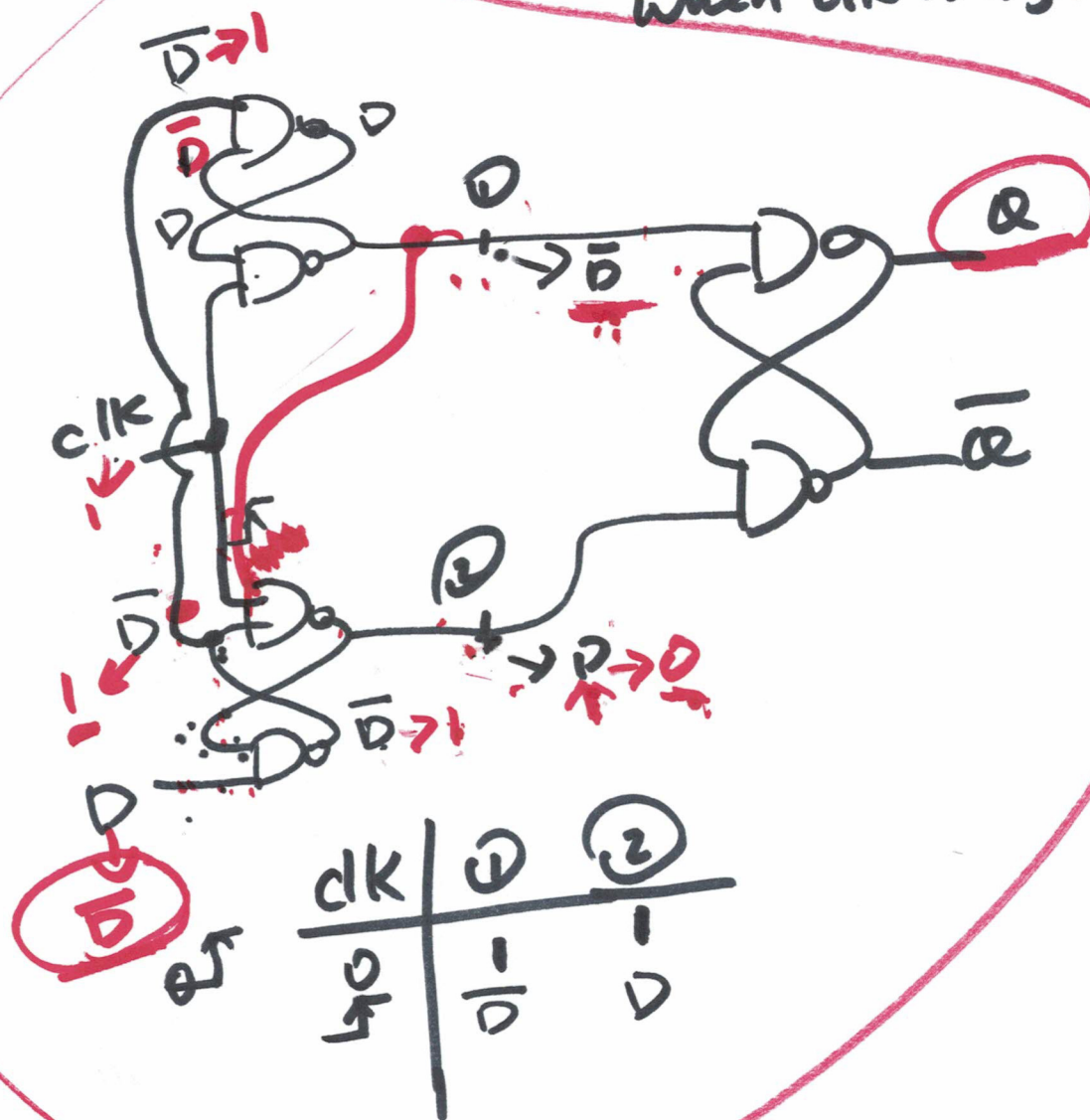


Asynchronous
DFF

③

T1 DFF

- $D \rightarrow Q$
- synchronous DFF
- Q remaining unchanged when clk is high if D changes



4

