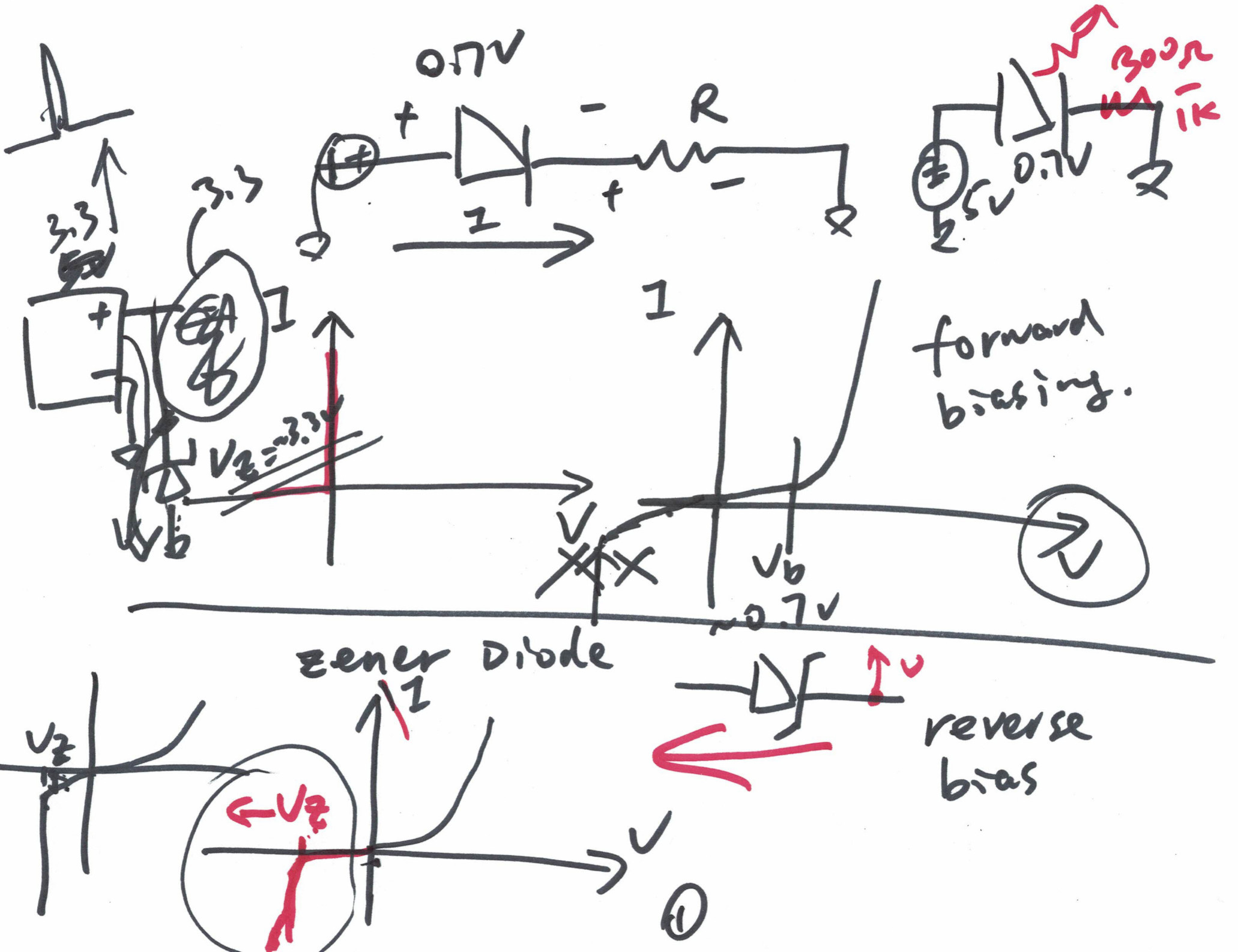
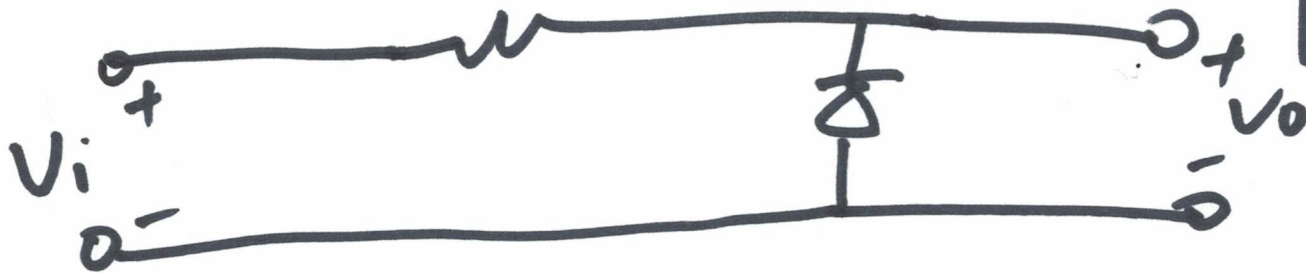
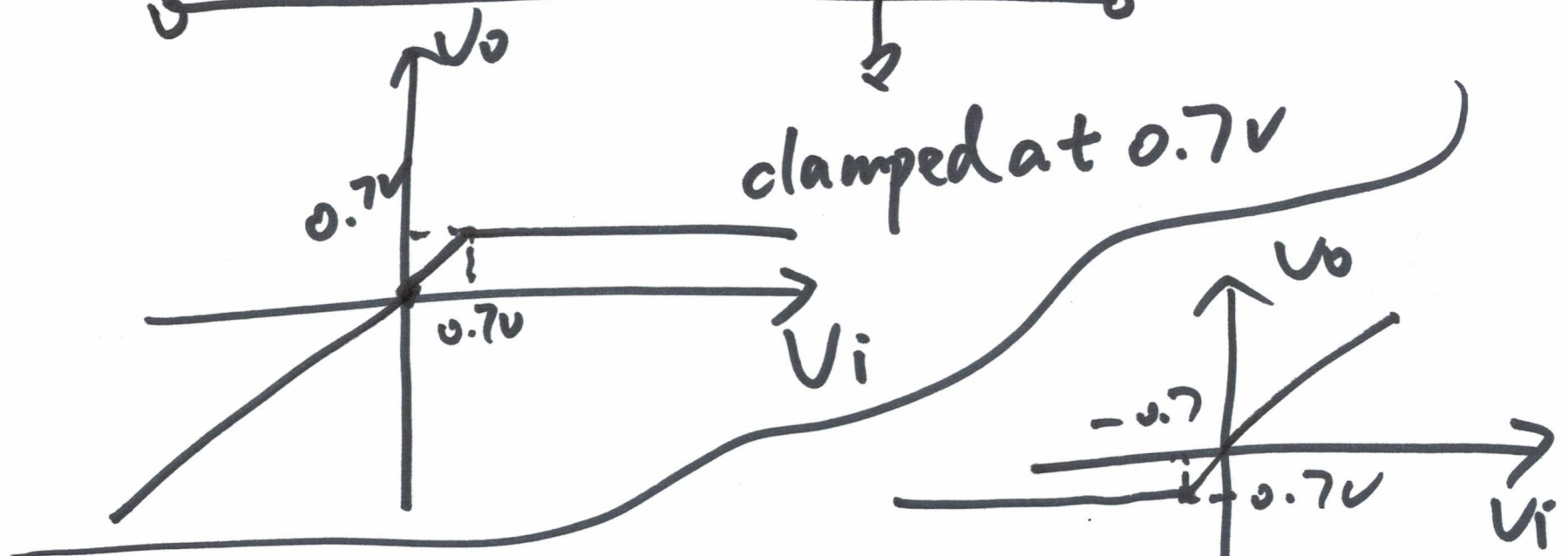
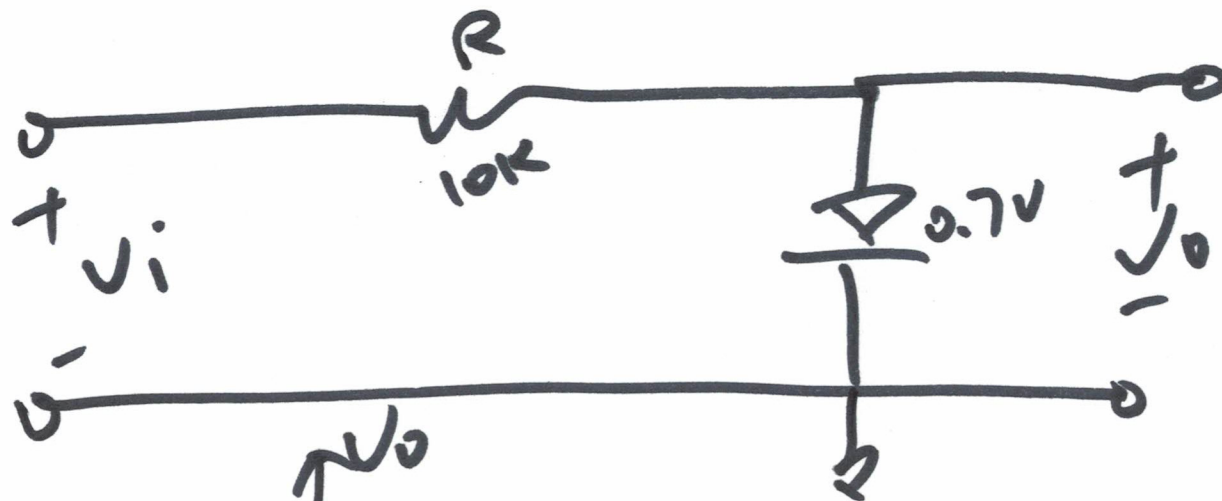
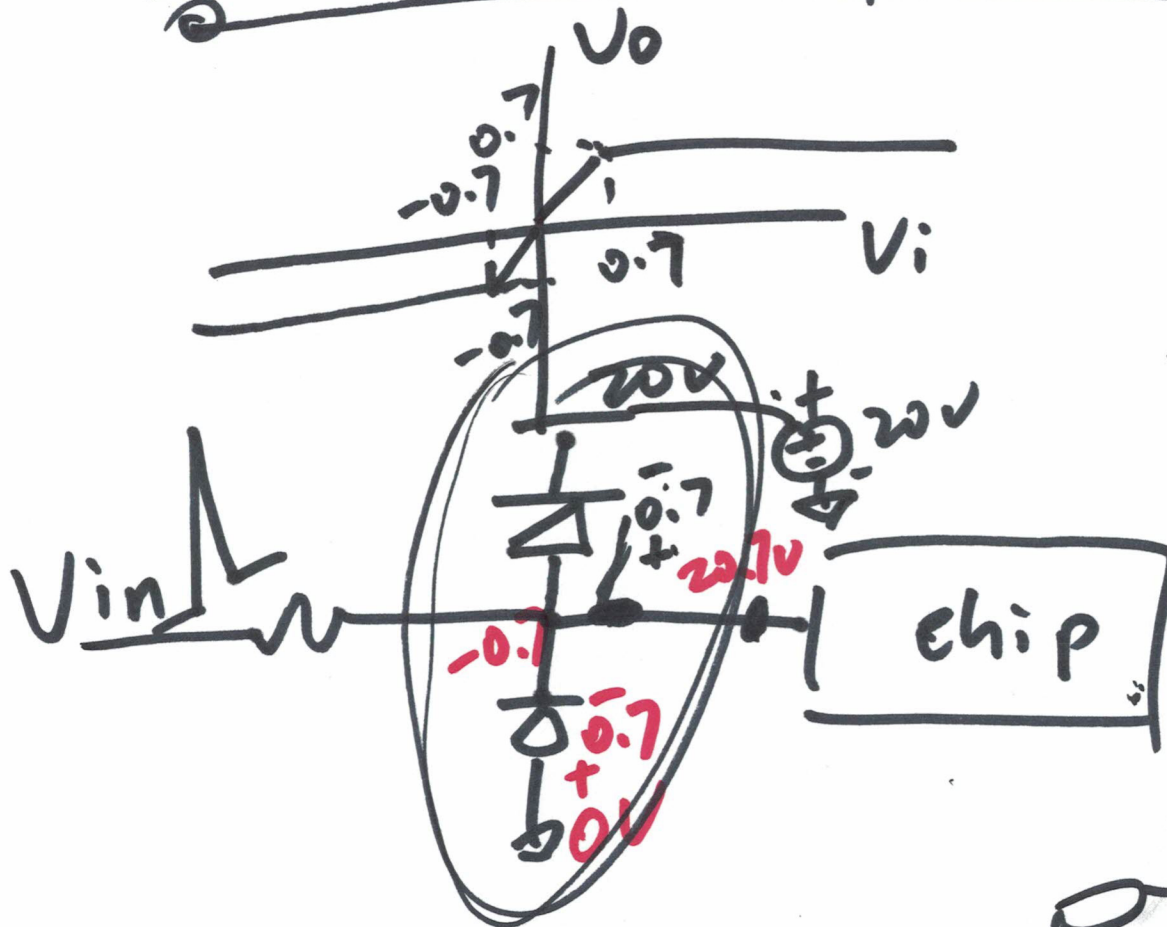
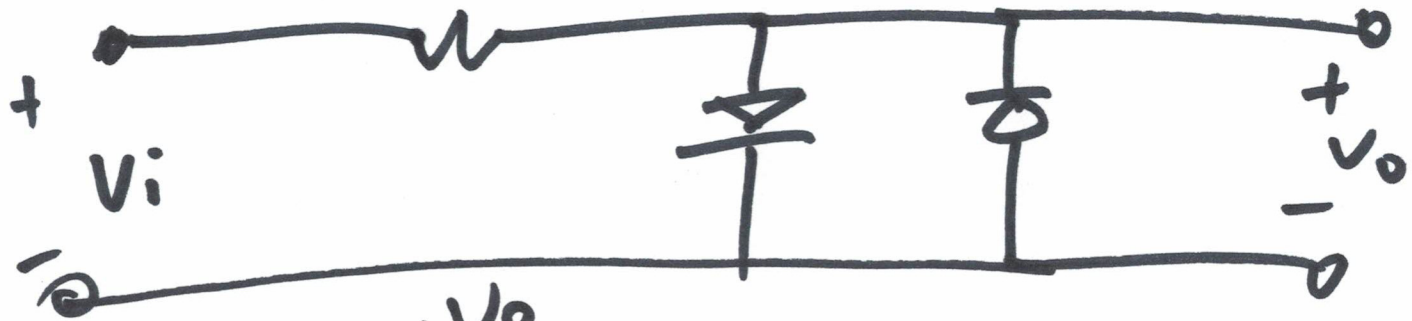






②



ESD protection

PDK
process
Design
20K kit

inv1 standard
inv2 cell library

(3)

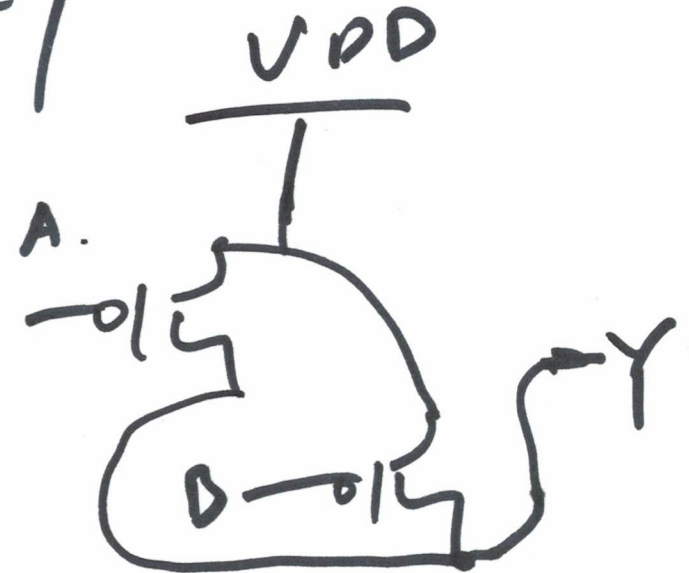
Static Logic Gates

① NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

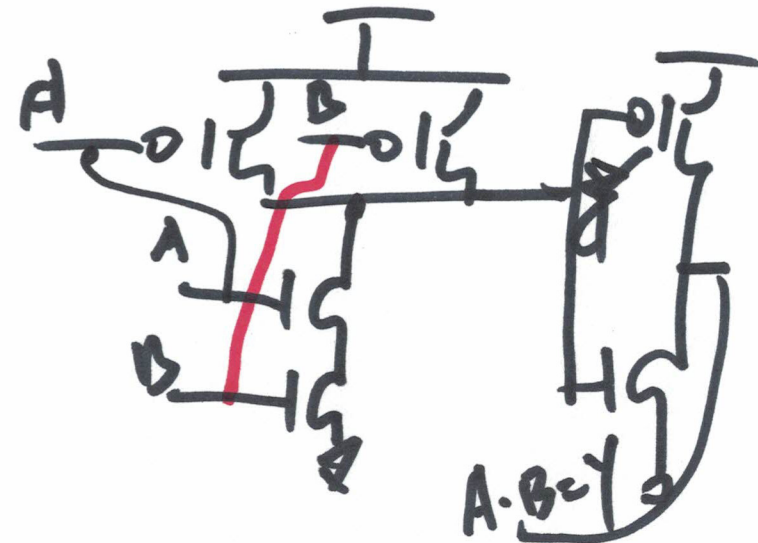
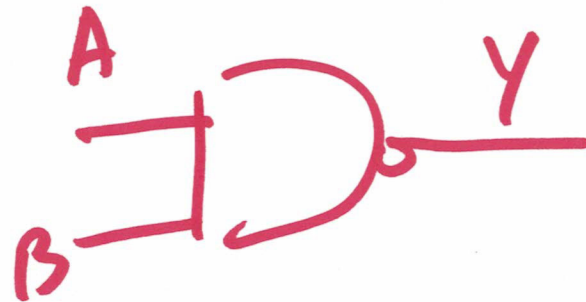
$\rightarrow$ pmos
 $\rightarrow$ nmos

$$\overline{A \cdot B} = Y$$



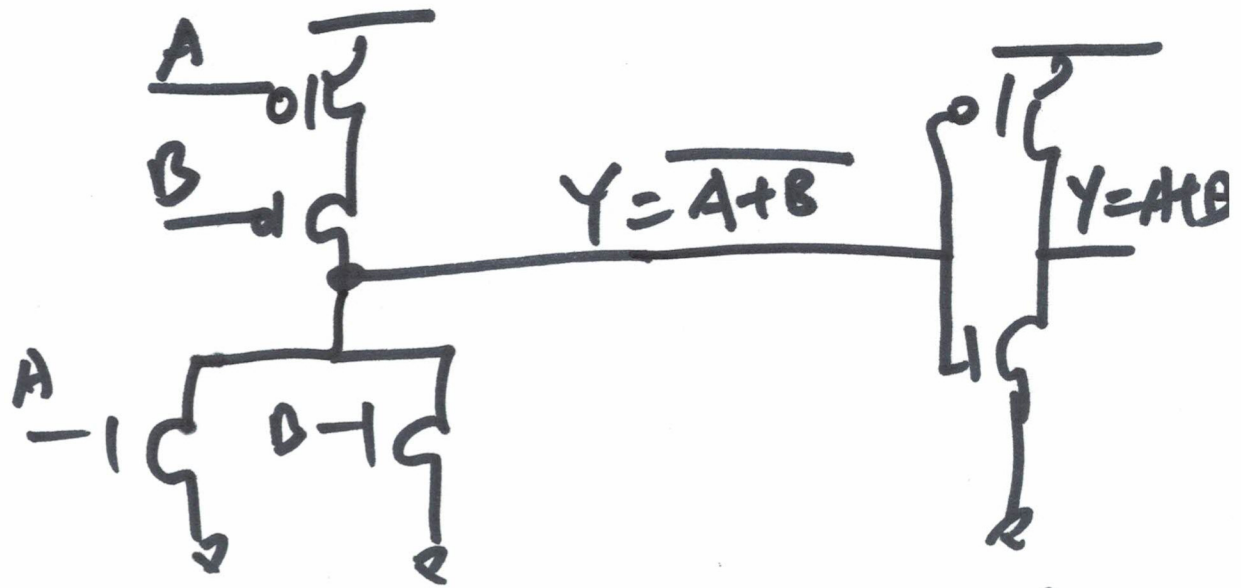
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND



④

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



$A + B + C$

