Square-Law Equations

For a triode-operating long-channel NMOS device

$$I_D = KP_n \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

for $V_{GS} \geq V_{THN}$ and $V_{DS} \leq V_{GS} - V_{THN}$

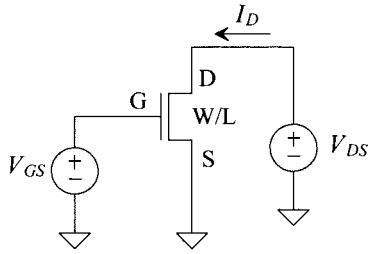
For a long-channel NMOS device operating in the saturation region:

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L}(V_{GS} - V_{THN})^2[1 + \lambda(V_{DS} - V_{DS,sat})]$$

for $V_{GS} > V_{THN}$ and $V_{DS} \geq V_{GS} - V_{THN}$

On the border between saturation and triode:

$V_{DS,sat} = V_{GS} - V_{THN}$ and the drain current is called $I_{D,sat}$, see Fig. 6.11



For the PMOS device equations make the following substitutions in the equations listed above

$$V_{DS} \rightarrow V_{SD},\ V_{GS} \rightarrow V_{SG}, \text{ and } V_{THN} \rightarrow V_{THP}.$$

All of the voltages and currents in the PMOS and NMOS equations are **positive**. For example, for the PMOS device to conduct a drain current requires $V_{SG} > V_{THP}$. For the NMOS to conduct a drain current requires $V_{GS} > V_{THN}$.