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On The Design of Low Power CMOS (SA-ADCs) for Biomedical Applications

By

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March 2016

Committee Page

On The Design of Low Power CMOS (SA-ADCs) for Biomedical Applications

By

TASNIM BASSAM SAMI NAZZAL

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in the Department of Electrical and Computer Engineering, University of Sharjah

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Signature of Author

Abstract

SUCCESSIVE APPROXIMATATION analog-to-digital converter (SA-ADC) is one of the most popular approaches for realizing A/D converters, due to its reasonably quick conversion time, moderate circuit complexity, high accuracy, and it's a proper choice for low power applications. Thus, one of the main challenges in designing SA-ADC is to succeed in proposing a low power, simple and accurate design.

This thesis presents three different CMOS realizations of an 8-bit successive approximation analog to digital converter (SA-ADC) for biomedical applications. The architecture of the proposed SA-ADCs consists of a sample and hold (S/H), a comparator, a successive approximation register (SAR) controller, and an 8-bit digital-to-analog converter (DAC). The proposed realizations are implemented using the same S/H circuit which is based on a sampling transistor with dummy switch, the choice of static or dynamic comparator, the choice of conventional or clock gated SAR, and the same binary weighted capacitor array single ended DAC based SAR architecture. In addition to that, the SAR controller is implemented using D-flip flop (D-FF) or hybrid latch-flip flop (HL-FF). The proposed SA-ADCs are presented, compared and simulated using 90nm CMOS technology file on LT-spice-IV.

The simulation results show that the SA-ADC realization which implemented by using the double-tail dynamic latched comparator and the clock-gated D-FF based SAR is superior from point of view of the power consumption. According to the simulation results, the low-power clock gated SA-ADC using D-FF realization consumes 200nW from 1V power supply without additional calibration or analog circuits. It has signal-to-noise ratio (SNR) of 53.8 dB, peak spurious-free dynamic range (SFDR) of 54.2 dB, and a signal-to-noise-and distortion ratio (SNDR) of 48 dB for a 250Hz full scale input sine wave. It has also an effective number of bits (ENOB) of 7.6-bits, and a figure of merit (FOM_2) of 0.1 pJ/Conversion-step. It achieves +0.34/-0.3 LSB and +0.79/-0.58 LSB of Differential non-linearity (DNL) and Integral non-linearity (INL) errors respectively.

Furthermore, the low-power clock gated SA-ADC using D-FF realization consumes 88.76 nW from 0.85V power supply without additional calibration or analog circuits. It has SNR, SFDR and SNDR of 54.6 dB, 39.19 dB and 37.92 dB respectively for the same input sinewave. It achieves ENOB of 6-bits with (FOM_2) of 0.13 pJ/Conversion-step. It has DNL and INL of +0.38/-0.28 LSB and +0.9/-0.85 LSB respectively.

Acknowledgment

First of all, I would like to express my deepest gratitude to our benevolent god, for bestowing upon me his grace and granting me the ability, the strength and the patience to complete my thesis after all the challenges and difficulties.

I take this opportunity to thank my supervisor Prof. Soliman Mahmoud, whose guidance has been instrumental in me having successfully presented this thesis and for his support through whole master study. I do sincerely thank Dr. Mohamed Shaker for the continuous support extended to me for solving some of the problems I faced in my thesis. I am also truly grateful to my committee members, Dr. Sohaib Majzoub and Dr. Lutfi Al Basha for their insightful suggestions and comments on my thesis.

I am indebted to my parents, Bassam and Hind, for their belief in my convictions, their patience, and for having provided me with all the necessary resources enabling me to achieve my goals. It was impossible for me to reach this level without their continued prayers. I sincerely thank my lovely sisters Saja, Hala and Aya with her husband Wasim and their daughter Sana who have been my mentor and source of inspiration in this project and for their continuous support. I would like to give my special thanks to my grandmother for her prayers which enabled me to complete my thesis. My sincere appreciation also goes to my uncle Basel for his care and continuous supports.

I would like to express my sincere gratitude to all my friends for the nice days I spent with them during my study and work period. Special thanks to Eng. Mohamed Buhatier for helping me in the MATLAB part of my thesis.

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Chapter 1

Introduction

With the continuous growth in technology, electronic devices are being improved to serve people's life in all aspects. As the number of people conducting sedentary life increases, chronic diseases are continuing to spread among people of all ages. One of the most important technology is developing biomedical systems for diagnosing, monitoring, and treating various diseases. Another important technology is the wireless applications. Handheld devices such as: cell phones, palmtop, and laptop computer are rapidly becoming an integral part of people daily lives. In most cases, these devices have compatible data communication interfaces by a cable connections and configuration procedures. An obvious solution is to get rid of these cables and use short range wireless links to facilitate on demand connectivity among devices.

This chapter introduces the thesis and it is organized as follows: Section 1.1 illustrates the thesis motivation. The thesis objectives are presented in section 1.2. Section 1.3 states the thesis contribution. Finally the thesis organization is included in section 1.4.

1.1 Thesis Motivation

The biomedical electronics world is rapidly changing with high future potential. With new technology, new designs with more features are placed into the biomedical devices. Nowadays, integrated circuit technology was developed in which the medical diagnostic systems can be miniaturized to portable devices. This kind of technology allow people to monitor their medical condition regardless of their age or location. For example, a recent study found nearly 90% of respondents are using mobile devices within their organizations to engage patients in their healthcare [1]. Furthermore, in large senior living facilities, the requirements of the care providers are fast and efficient ways to collect the residents' health data and update patient records in real time [1]. A small mobile device such as a smartphone or tablet are preloaded with healthcare applications and it consists of mobile healthcare sensor, device, server and medical service which make it possible to perform these tasks easily from any location. Various biomedical signals will be sensed by the sensor such as: sleep monitoring, heart rate, skin temperature, stress,

electrocardiogram and blood pressure. After that, these biomedical signals will be transferred to the server by the device which will stored and analyzed it. An additional benefit of this approach is such devices can be secured and controlled remotely via medical service [1].

Analog-to-digital converter (ADC) is considered as one of the main electronic blocks in the biomedical systems and healthcare integrated circuit. It becomes a bottleneck in data processing applications and it limits the performance of the overall system. Low power design and high resolution ADC are the main requirements in the biomedical applications. Sigma-delta ADC is a proper choice for high resolution ADC where the successive approximation analog to digital converter (SA-ADC) is a proper choice for low power ADC [2].

1.2 Thesis Objectives

The objective of this thesis is to search and find out low power 8-bit SA-ADC for portable biomedical applications. The architecture of the SA-ADC used in this work is single ended DAC based and it consists of a sample and hold (S/H) circuit, a comparator, a successive approximation register (SAR) controller in addition to digital to analog converter (DAC) as shown in Figure (1.1) [3]. The analog to digital conversion is based on the binary search algorithm. At the sampling phase, the sample and hold (S/H) circuit stores the analog signal. The comparator determines the polarity of the difference between the reference voltage and the sampled analog signal. After that, the comparator output triggers the successive approximation register (SAR) controller which feeds the digital to analog converter (DAC) to prepare the reference voltage for the next comparison. In this algorithm, each bit needs one clock cycle to be determined. Therefore, the SA-ADC needs n clock cycles to complete an n-bit conversion [3].

The most power efficient SA-ADC is derived from three different possible realizations. These realization are implemented using the same S/H circuit which is based on a sampling transistor with dummy switch, the choice of static or dynamic comparator, the choice of conventional or clock gated SAR, and the same binary weighted capacitor array DAC. In addition to that, the SAR controller is implemented using D-flip flop (D-FF) or hybrid latch-flip flop (HL-FF). The low power dissipation is behind the use of the simplest S/H and DAC circuits without additional calibration or analog circuits. The first realization is implemented using static comparator and conventional SAR, the second realization is implemented using static comparator and clock gated

SAR and the third realization is based on the double-tail dynamic latched comparator and clock gated SAR. These realizations are characterized by moderate speed, moderate accuracy, and low power dissipation which meets the requirements of biomedical applications [2]. The proposed SA-ADCs are simulated and compared using 90nm CMOS technology file on LT-spice-IV.

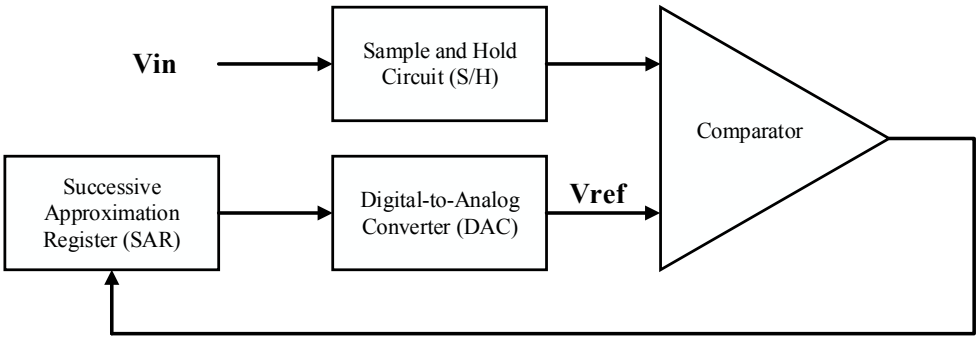


Figure (1.1) Block diagram of a single ended DAC based SAR ADC architecture [3]

1.3 Thesis Contribution

The fundamental building blocks of the SA-ADC are S/H circuit, comparator circuit, DAC circuit and SAR control logic. The comparator circuit is one of the main sources of power consumption in the SA-ADC for low frequency applications. The choice of the static or dynamic comparator structure has a great effect on the power consumption [2,4]. Furthermore, the SAR control logic is considered a source of dynamic power consumption as a digital circuit due to its high frequency clock signal [2,5].

In this thesis, a survey of different structures and design considerations of each building block in the SA-ADC has been studied, analyzed, simulated and compared in order to select the best candidate for biomedical (low-frequency) applications in term of low power consumption. As a result, three different CMOS realizations of an 8-bit single ended DAC based SAR ADC are proposed. Moreover, they are implemented using alternative building blocks of the SA-ADC in order to illustrate the effect of each building block structure on the SA-ADC performance especially on the power consumption. The aim is to reduce the power consumption. Therefore, in each realization the power consumption has been minimized using alternative building blocks.

The second main contribution in this thesis is that, the SAR controller for each realization is implemented twice, the first one using D-flip flop (D-FF) and the second one using the hybrid latch-flip flop (HL-FF) in order to illustrate the effect of the flip flop (FF) type on the power consumption of the SA-ADC. It was worth to note that the structure's choice of each building blocks in the SA-ADC is not the only way to achieve minimum power consumption, but the suitable type of the FF should be selected in order to save a great amount of power consumption regarding the FF complexity.

The proposed realizations are simulated using 90nm CMOS technology file on LT Spice IV under supply voltage of 1V. The simulation results show that the SA-ADC realization which implemented by using the double-tail dynamic latched comparator and the clock-gated D-FF based SAR without additional calibration or analog circuits is superior from point of view of the power consumption compared with the first two realizations given in this thesis and also compared with previous work given in [2,6,7,8,9]. A layout and extraction of the best realization in term of power consumption is done using L-edit. In addition to that, it was tested under supply voltage of 0.85 V to achieve further reduction in power consumption. A reconstruction of the real recorded electroencephalogram (EEG) signal was realized for the best realization under 1V supply voltage and it was consistent with the input of the real recorded EEG signal waveform.

1.4 Thesis Organization

This thesis is organized into six chapters with references and appendix listed at the end. Each chapter has a brief introduction of the work undertaken and it is followed by the detailed analysis.

Chapter 2 illustrates a survey of sample and hold (S/H) circuits, which is the first block in the SA-ADC. It introduces different structures of S/H circuits which meet the requirements of low and high frequency applications. A simulation was done for the introduced S/H circuits in low, medium and high frequency and the best S/H circuit has been chosen for the biomedical signals.

Chapter 3 reviews the comparator circuits which is the second block in the SA-ADC. It was simulated and tested in low, medium and high frequency. As a result of this chapter, a low power dynamic comparator has been chosen for the biomedical signals.

In Chapter 4, different topologies of digital-to-analog converters (DACs) have been discussed. The advantages and disadvantages of each DAC have been illustrated. A suitable DAC has been chosen and simulated for the biomedical signals.

Chapter 5, illustrates two different successive approximation register (SAR) controllers which are the conventional SAR and clock gated SAR. After these two controllers have been studied, a simulation and a comparison were performed on the two SAR controllers. Furthermore, they were tested on D-FF and HL-FF. The best SAR controller in term of power consumption has been selected.

The complete CMOS realizations of an 8-bit SA-ADC and simulation results are illustrated in Chapter 6. It shows the SA-ADC architecture using different ways to realize its key building blocks result in three proposed possible realizations of an 8-bit SA-ADC. These realizations are discussed, simulated and compared to figure out the best candidate from power consumption point of view and achieving reasonable performance metrics. In addition to that, these proposed realizations have been compared with previous works in this chapter. Furthermore, this chapter presents a layout and reconstructed of a real recorded EEG signal as an example of one of the biomedical signals for the best proposed realization in term of power consumption. Also, it includes the best low power realization simulation results under supply voltage of 0.85 V.

Finally, Chapter 7 offers conclusions and recommends some possible future work that may be undertaken in the same direction.

Chapter 2

Sample and Hold Circuits

2.1 Introduction

Sample-and-hold (S/H) circuit is one of the main significant analog building blocks, especially in analog-to-digital converters (ADCs) [3]. It is also often referred to as "track-and-hold" circuit. Normally, these two terms are synonymous except for a few individual switched capacitor sample and hold circuits that do not have a phase where the output signal is tracking the input signal. It is the first block of the ADC components in which the input signal is seen by the input of the S/H circuit. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system. In many cases, using the S/H circuit at the front of the data converters have a significant effect. This effect appears in minimizing the errors due to slightly different delay times in the internal operation of the converter [3].

There are many types of S/H circuits; the first type is S/H circuits with an active block (like the operational amplifier) and/or supply voltage which includes S/H circuit with clock feedthrough cancellation, inverting S/H circuit and S/H circuit with bootstrapped technique. The second type is S/H circuits without an active block and does not need a supply voltage [3].

The objective of this chapter is to select the best S/H circuit candidate for each application among the introduced types under low voltage operation. The introduced S/H circuits are using either one single sample transistor or transmission gate, bootstrapped switch or not and single ended structure or differential. The reliability and accuracy of the S/H circuit depend mainly on the on-resistance of the sampling switch which will affect the switch linearity. It's worth noting that different sampling rates are used for different applications. This will affect the signal to noise and distortion ratio (SNDR), speed and power consumption of the S/H circuit and the overall ADC. Depending on the application, the emphasis will be on different metrics. In addition to that, a simulation was done for the presented S/H circuit types using 90nm CMOS technology on LT Spice IV. Furthermore, they were tested in low (250 Hz), medium (20 KHz), and high (1 MHz, 7 MHz and 13.6 MHz) frequency input signals in order to select the best S/H circuit candidate for each application. This chapter is organized as follows: Section 2.2 illustrates basic S/H circuit and

its modified versions without bootstrapped techniques. S/H circuits with bootstrapped techniques are presented in section 2.3. Section 2.4 introduces proposed modified low-power bootstrapped S/H circuit using transmission gate and section 2.5 includes simulation results for different applications.

2.2 Basic Sample and Hold Circuit

Basic S/H circuit is considered one of the simplest S/H circuits that can be realized using a CMOS technology [3]. This section introduces basic S/H circuit architecture, its problems, and a modified versions of it which compensate the induced problems. All the presented S/H circuits in this section are from the second type of S/H circuits.

Basic S/H circuit is a single-ended architecture. It consists of single NMOS switch M_1 and a sampling capacitor C_s as shown in Figure (2.1). It operates in a single phase Ø. When Ø goes high the transistor turns ON, and the voltage across the capacitor ($V_{out,sampled}$) follows the input voltage (V_{in}). When Ø goes low, the transistor turns OFF, and ($V_{out,sampled}$) will stay constant having a value equal to (V_{in}) at the instance of Ø went low [3].

A simulation was done for this circuit for an electrocardiogram (ECG) signal properties [2]. The input signal is a sinusoidal input with amplitude and frequency of 500 mV_{p-p} and 250 Hz respectively. This signal is sampled at clock frequency of 10 KHz. The sampling capacitor C_s is chosen to be 5pF. It is worth noting that the value of the sampling capacitor is a function of two main factors: the ADC input range and resolution, which translates into an equivalent thermal noise specification ($\frac{KT}{C_s}$) [2]. The aspect ratio of the transistor M_1 is (W=540nm / L=90nm). Figure (2.2) shows the sampled output voltage ($V_{out,sampled}$) of this circuit. All the introduced types have the same ($V_{out,sampled}$) shape and the main difference between them will be illustrated in the simulation results section. The noise spectrum of this circuit was calculated over the interest bandwidth of 500 Hz as shown in Figure (2.3) with total RMS output noise of 26.58 µV.

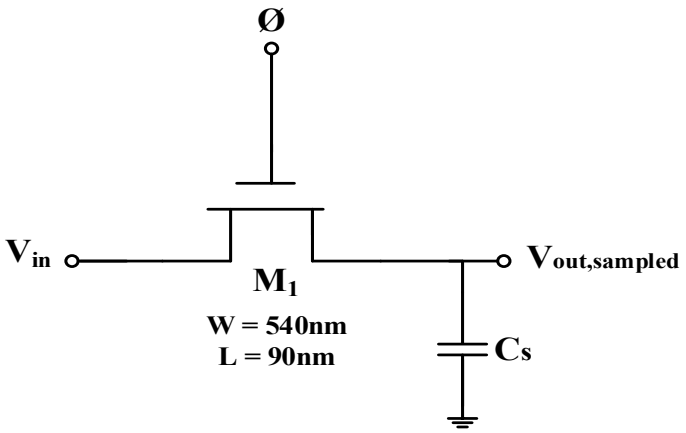


Figure 2.1 Basic sample and hold circuit [3]

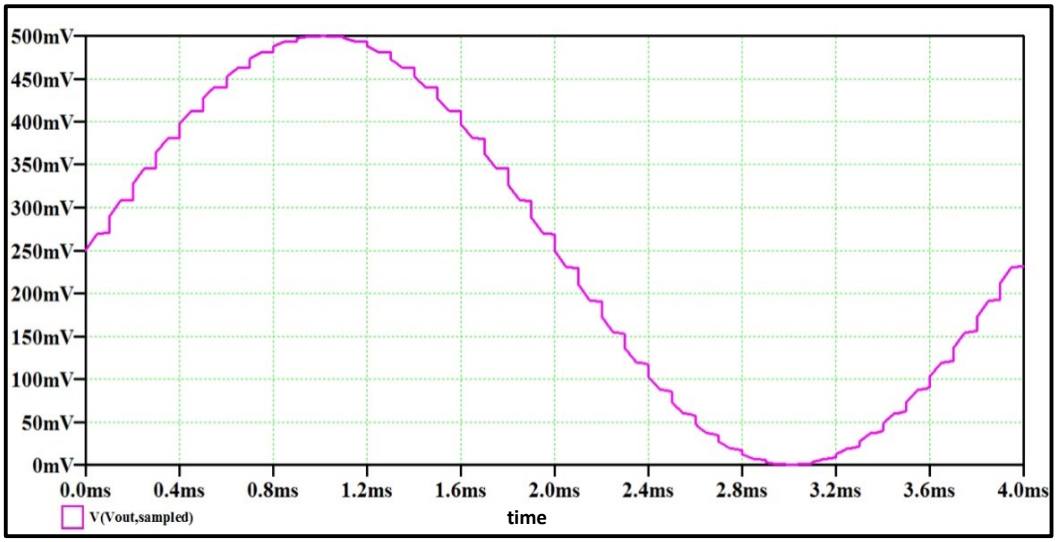


Figure 2.2 Sampled output Voltage ($V_{out,sampled}$) with sampling frequency of 10 KHz

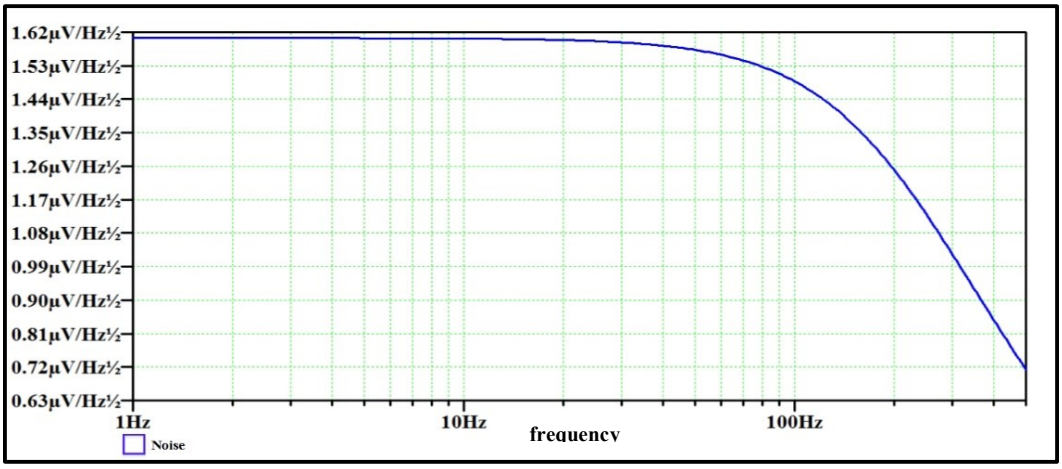


Figure 2.3 Noise spectrum of ($V_{out,sampled}$) over bandwidth of 500 Hz

Charge injection and clock feedthrough are considered two major problems occur in basic S/H circuit. It is happening when a transistor is used as a switch in a switched capacitor circuit [2,3]. A modified versions of basic S/H circuit will be introduced in the following subsections in order to reduce the effect of these problems and compensate the induced errors.

Charge injection occurs when the clock Ø goes high. The NMOS transistor turns ON, and the input voltage is sampled by the capacitor C_s. Due to the inverted channel, a charge under the gate oxide is produced, and it is given as follows [2]:

$$Q_{ch} = W\ L\ C_{ox}\ (V_{DD} - V_{in} - V_{tn}) \tag{2.1}$$

Then, when the clock Ø goes low, The NMOS transistor turns OFF. The created channel charge will flow out from the NMOS gate into its source and drain creating an error in the sampled voltage. If all the charges are injected on the sampling capacitor C_s, the sampled output voltage is given by the following equation [2]:

$$V_{out} = V_{in}\left(1 + \frac{W\ L\ C_{ox}}{C_s}\right) - \left(\frac{W\ L\ C_{ox}}{C_s}\right)(V_{DD} - V_{tn}) \tag{2.2}$$

Therefore, the sampled output voltage is affected by two parameters. These parameters are a non-unity gain $\left(1 + \frac{W\ L\ C_{ox}}{C_s}\right)$ and a constant offset voltage $\left(- \left(\frac{W\ L\ C_{ox}}{C_s}\right)(V_{DD} - V_{tn})\right)$ [2].

Clock feedthrough is defined as the coupling between the clock transitions and the sampling capacitor by the MOS transistor through its gate-drain or gate-source overlap capacitances. When the clock Ø goes high, an overlap capacitance is fed through the gate-source, the gate-drain, or both. While in the OFF state of the transistor, a capacitive divider is created. This operation result in an offset voltage which is given as follows:

$$\Delta V_{offset} = \frac{C_{ov}}{C_{ov} + C_s}\ V_{DD} \tag{2.3}$$

Where C_{ov} is the overlap capacitance [2].

2.2.1 Differential Basic Sample and Hold Circuit

The principle of this circuit is to cancel the charge injection problem by applying a differential balanced input on the basic S/H circuit as shown in Figure (2.4). This is done if the differential sampling capacitors C_{s1} and C_{s2} are matched [10]. A simulation was done for this circuit using the aspect ratios which are illustrated in Figure (2.4) with C_{s1} and C_{s2} of 5pF and the same previous input characteristics. Figure (2.5) shows the input clock pulses. The differential input and differential output are shown in Figure (2.6) and Figure (2.7) respectively. Figure (2.8) shows the noise spectrum of the differential output with total RMS noise of 29 µV.

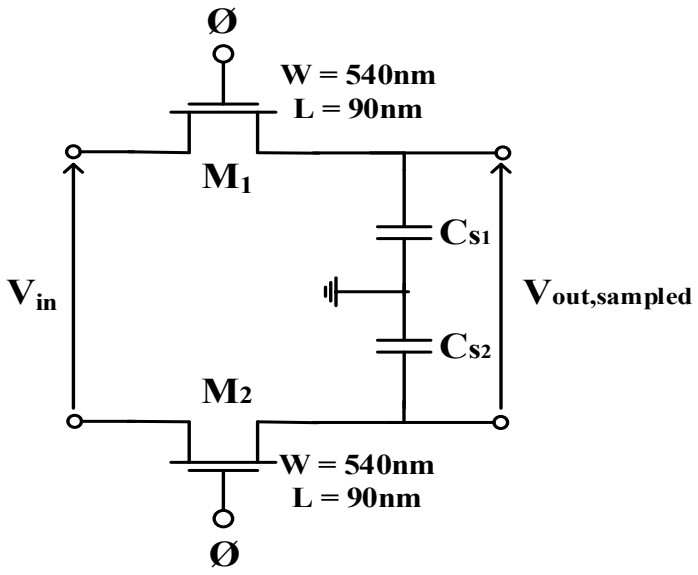


Figure 2.4 Differential basic sample and hold circuit [10]

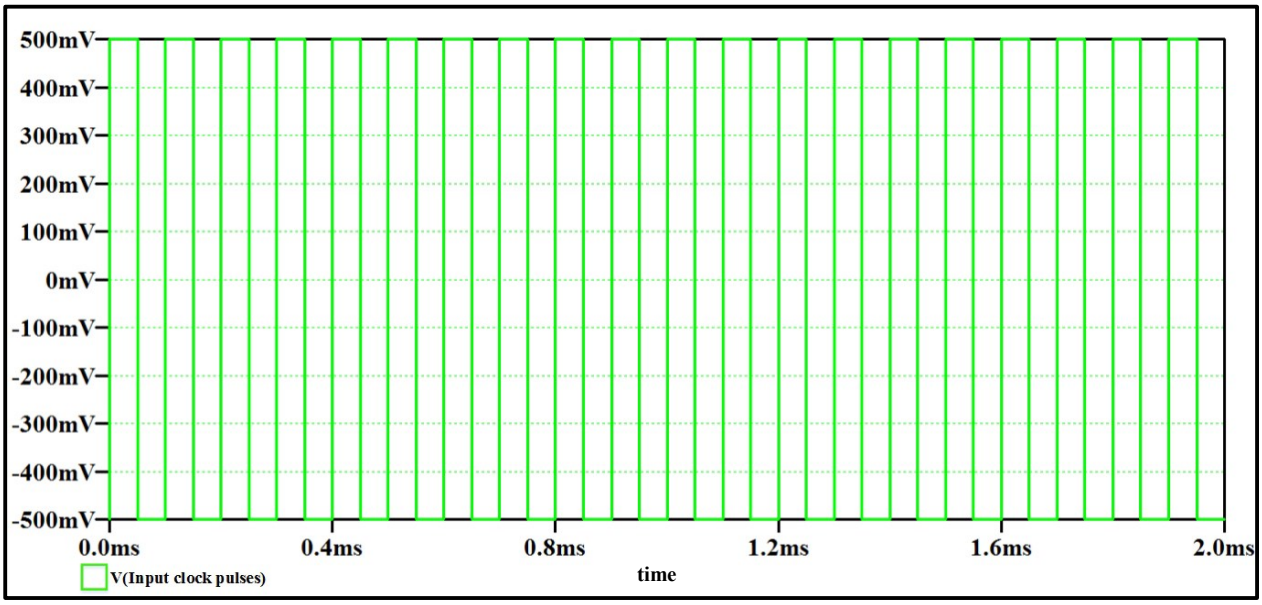


Figure 2.5 Input clock pulses (Ø)

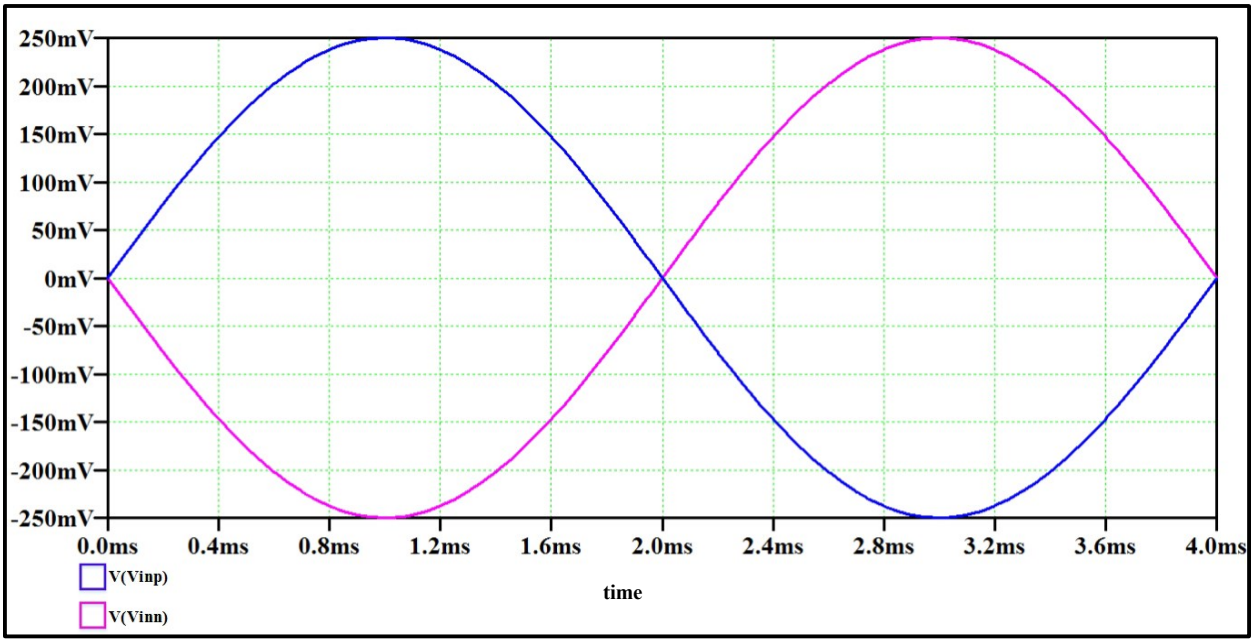


Figure 2.6 Differential balanced input

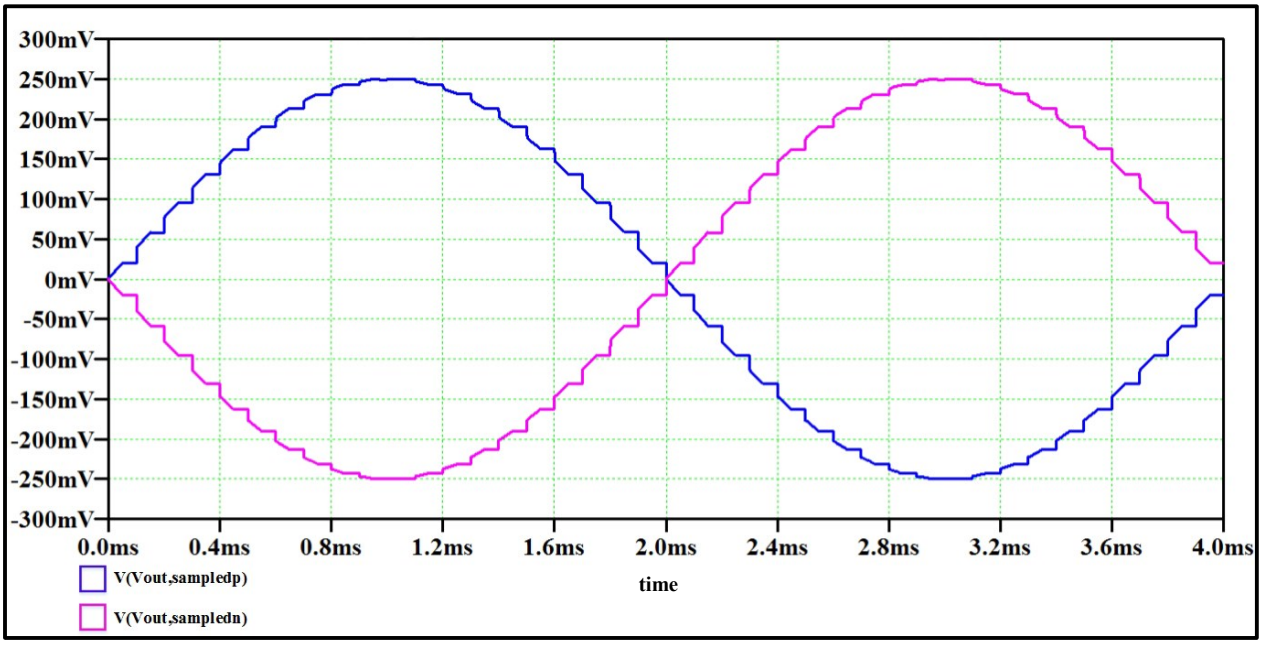


Figure 2.7 Differential output

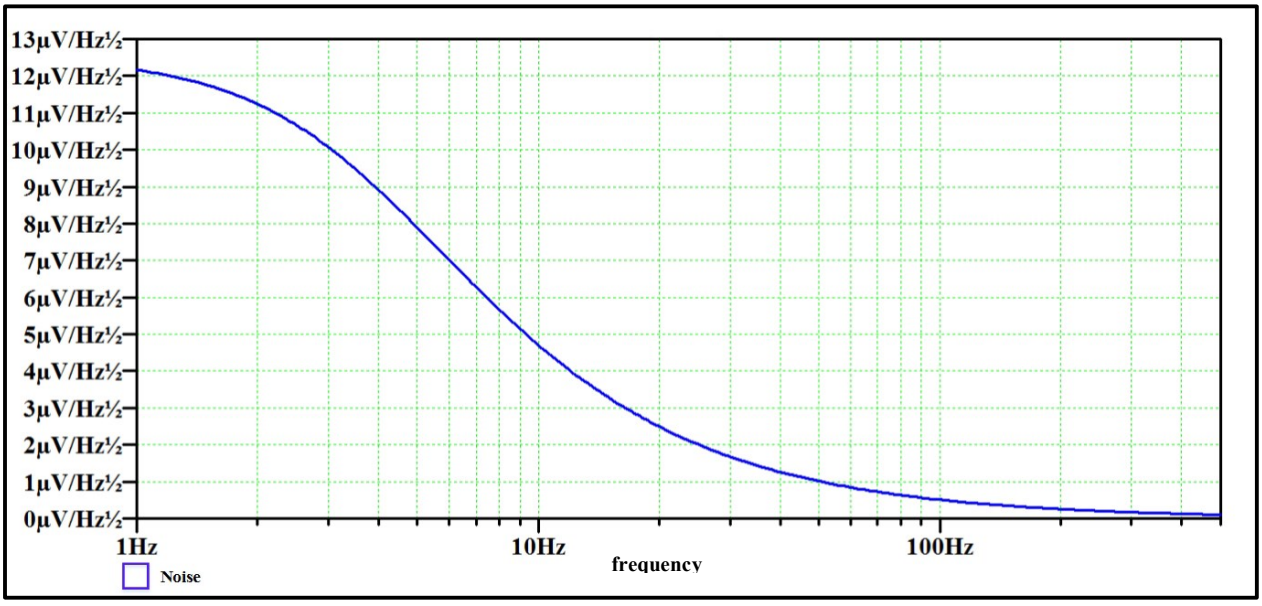


Figure 2.8 Noise spectrum of differential output over bandwidth of 500 Hz

2.2.2 Basic Sample and Hold Circuit with Dummy Switch

This method is considered one of the most common methods that is used to overcome the charge injection and clock feedthrough effect. Figure (2.9) shows basic S/H circuit with dummy switch. M_2 is a dummy switch with its source and drain shorted. It is placed in series with M_1 having a complement clock of Ø. When M_1 turns OFF, and M_2 turns ON, M_2 will absorb the channel charge deposited on C_s. The following equations express the injected charge Δq_1 and the absorbed charge Δq_2 respectively as follows [2]:

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}(V_{DD} - V_{in} - V_{tn1})}{2} \quad (2.4)$$

$$\Delta q_2 = W_2 L_2 C_{ox}(V_{DD} - V_{in} - V_{tn2}) \quad (2.5)$$

In order to achieve ($\Delta q_1 = \Delta q_2$), the channel width of M_2 should be half that of M_1 assuming the channel length of both transistors is equal. Thus, the charge injection and clock feedthrough will be suppressed [2]. A simulation was done for this circuit using the aspect ratios which are illustrated in Figure (2.9) with C_s of 5pF and the same previous input characteristics. It has the same noise spectrum as the basic S/H circuit with total RMS output noise of 26.57 µV.

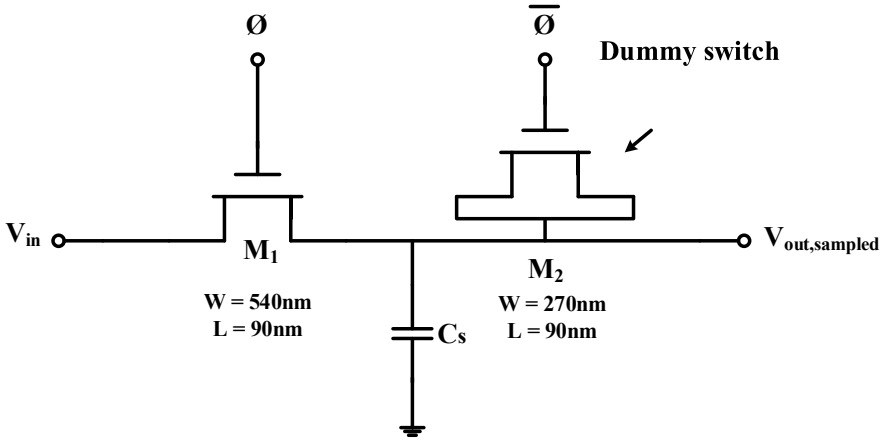


Figure 2.9 Basic sample and hold circuit with dummy switch [2]

2.2.3 Basic Sample and Hold Circuit using Transmission Gate

This technique is based on replacing the single transistor in Figure (2.1) with a CMOS transmission gate as shown in Figure (2.10). If the size of PMOS transistor M_P is taken to be the same as NMOS transistor M_N. Then, the charge injection due to each transistor will be canceled when the transmission gate turns OFF. PMOS transistor M_P have the advantage in enhancing the on-conductance between the input and output when the input is close to the supply voltage [3,11]. A simulation was done for this circuit using the aspect ratios which are illustrated in Figure (2.10) with C_s of 5pF and the same previous input characteristics. It has the same noise spectrum as the basic S/H circuit with total RMS output noise of 26.59 μV.

However, at the circuit level, in low voltage and high frequency condition; the MOSFETs switches may not be fully turned on as they are under a higher voltage operation. It is happening when the sum of the absolute value of the PMOS threshold voltage and that of the NMOS is greater than the supply voltage. The MOSFETs switches may now have extremely poor conductance and would limit the bandwidth of the circuits. Therefore, a bootstrapped technique is required [11].

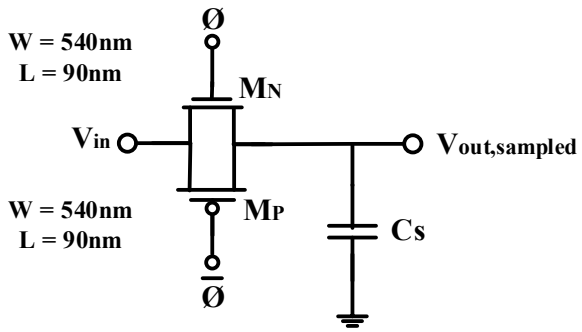


Figure 2.10 Basic sample and hold circuit using transmission gate [3]

2.3 Sample and Hold Circuits with Bootstrapped Technique

Two types of bootstrapped techniques have been introduced in this section [11,12]. The first type keeps the on-resistance of the sampling switch small and varying due to the gate-source voltage variation of the sampling switch which is S/H circuit with boosted driver technique [11,13]. The second type keeps the on-resistance of the sampling switch small and constant because the gate-source voltage of the sampling switch is constant and independent of the input signal which is S/H circuit with bootstrapped technique [12]. These techniques are convenient in low voltage operation. They aims to provide a small on-resistance of the sampling transistor which results in improving the switch linearity, reliability and bandwidth with high signal-to-noise and distortions ratio (SNDR) [11].

2.3.1 Sample and Hold Circuit with Boosted Driver Technique

Figure (2.11) shows S/H circuit with boosted driver using transmission gate. The goal of this circuit is to achieve both low power and a wide bandwidth. The gate of the transistor M_N is connected to the boosted driver output. It operates by applying a square wave input signal of (V_{DD}). When Ø is high, the bottom plate of C_2 and the top plate of C_1 are charged to (V_{DD}). When Ø goes low, the supply voltage is applied to each second capacitor plates. Then, the charge stored in C_2 is transferred to the gate of M_N by M_3 with an inverted square wave output which is generated according to:

$$V_{gateM_N} = 2V_{DD} \cdot \frac{C_2}{C_{gateM_N} + C_2 + C_{parasitic}} \qquad (2.6)$$

In other words, the boosted driver output has a periodical signal switching between ($2V_{DD} - \Delta V$) and the ground. (ΔV) result from the charge sharing between the capacitor C_2 and the parasitic capacitance at the gate of M_N. The bandwidth of this circuit is ($1/2\pi R_{on} C_s$), where R_{on} the on-resistance of the sampling switch M_N. In this technique, the on-resistance of the sampling switch is small and varying due to (V_{GS}) variation [11,13]. For the same input signal that is mentioned previously with supply voltage (V_{DD}) of 1V. Figure (2.12) illustrates the simulation results of the input clock pulses. C_1, C_2 and C_s are chosen to be 2pF, 2pF and 5pF respectively. The transistors

aspect ratios' are illustrated in Figure (2.11). Figure (2.13) shows zoomed ($V_{out,sampled}$) of this circuit with the inverted square wave signal switching between 2V and the ground is formed on the gate of M_N (boosted clock). It has the same noise spectrum as the basic S/H circuit with total RMS output noise of 26.59 μV.

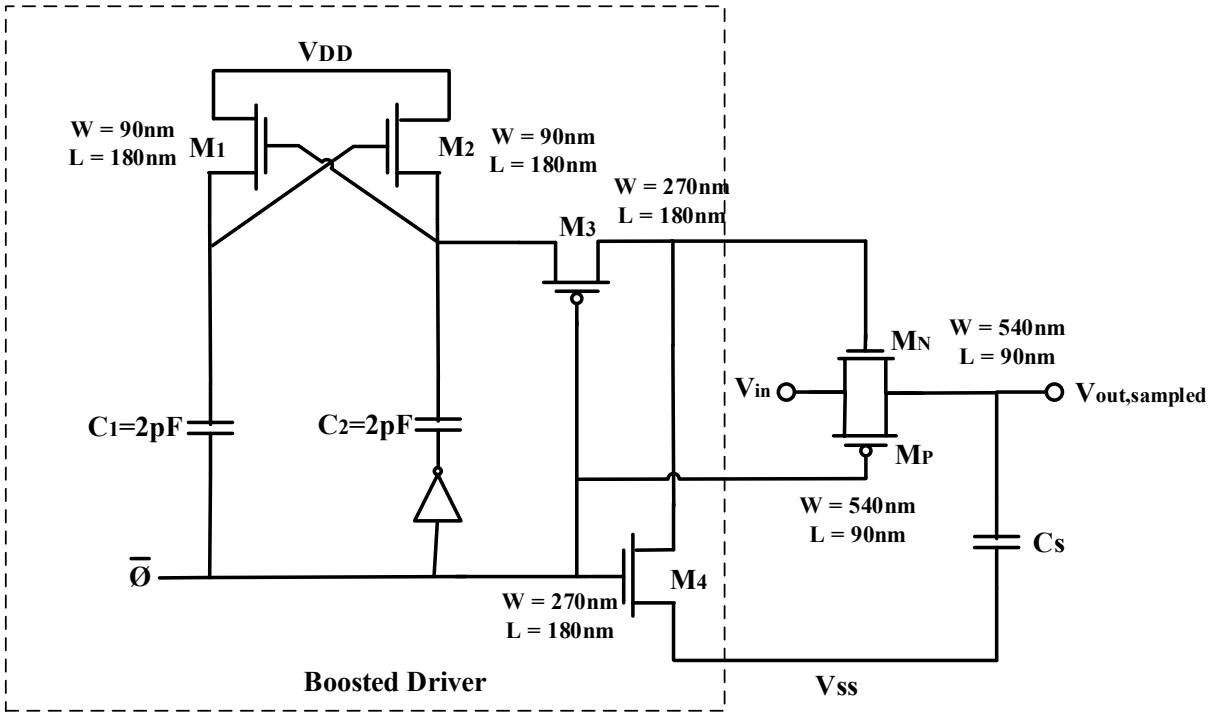


Figure 2.11 Sample and hold circuit using transmission gate with boosted driver [11]

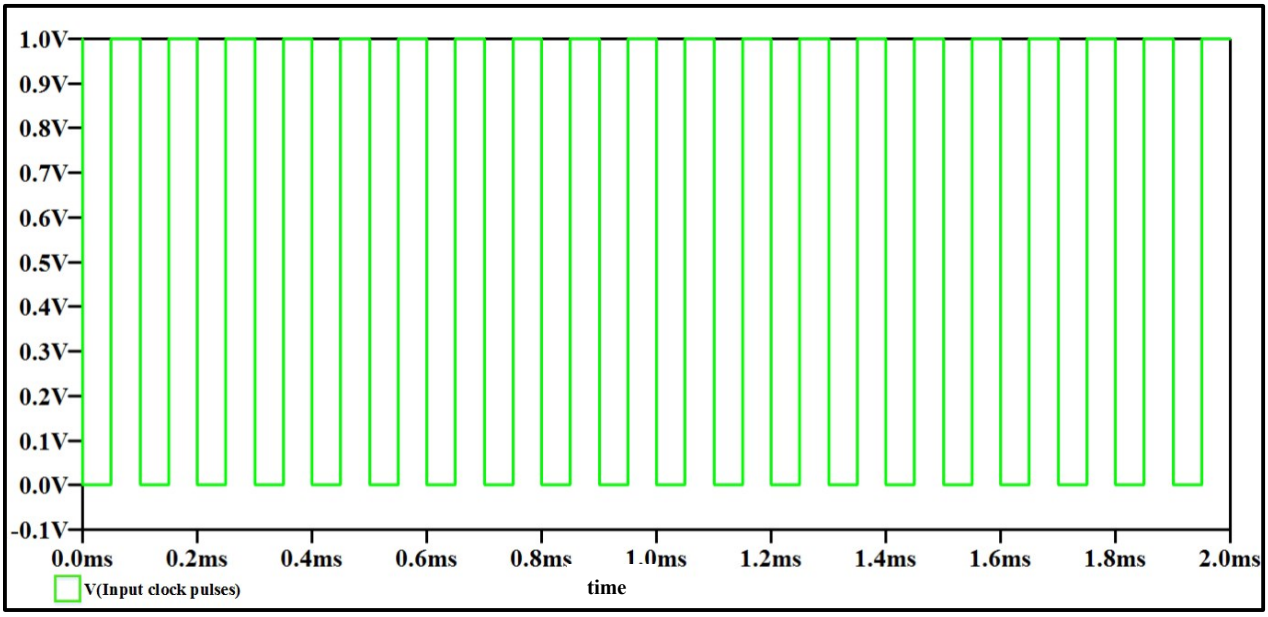


Figure 2.12 Input clock pulses (Ø)

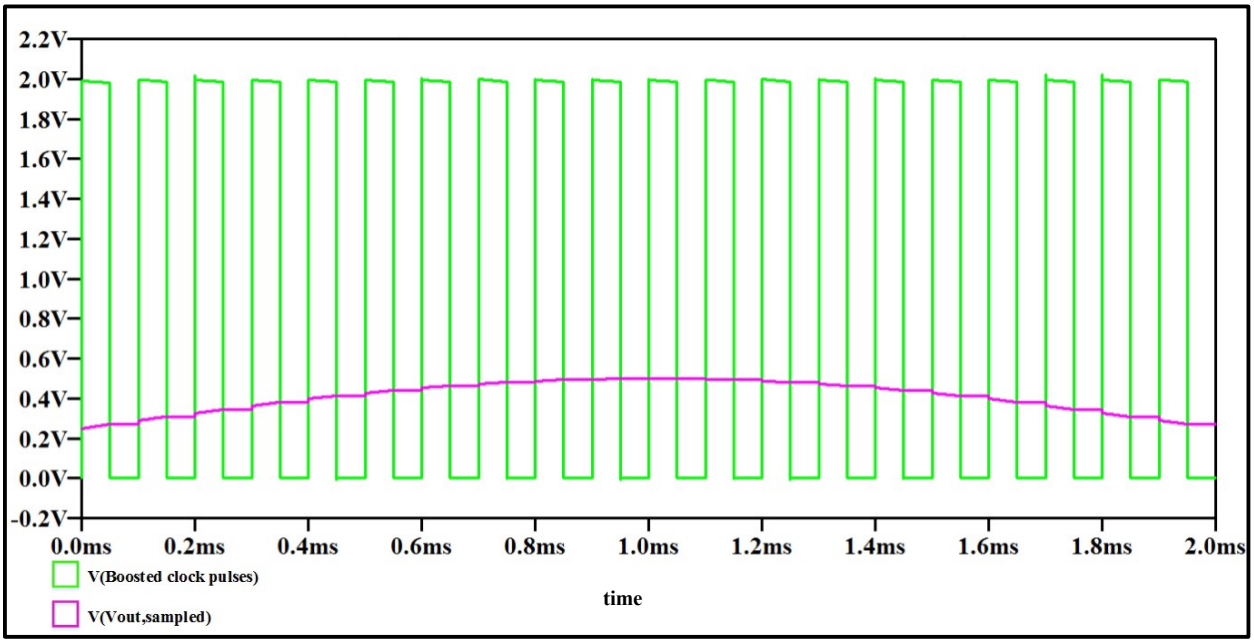


Figure 2.13 Zoomed ($V_{out,sampled}$) with inverted boosted clock

2.3.2 Sample and Hold Circuit with Bootstrapped Technique

In low voltage operation, the reliability constraints of the technology must not be crashed. For example, using MOS transistor as a switch in low voltage operation has several disadvantages. As a result of decreasing the supply voltage, the threshold voltage of high-threshold transistors must be reduced. This will increase the sub-threshold leakage current exponentially which distort the analog sample, and hence increase the static power dissipation. In another technique, MOS transistors with high-threshold voltage are used. This technique has disadvantages in which the transistors have high series resistance which reduce the speed [12].

However, the consumer trends goes for high performance portable electronics. Magnify the importance of the power dissipation reduction to guarantee longer battery life for enhanced portability and noise reduction for high signal integrity. Therefore, long circuit lifetime can be assured with great confidence by keeping the device voltages within the rated supply voltage. This can be observed by implementing the MOS switches without low-threshold devices by using a bootstrapped technique which does not subject the devices to large terminal voltages [12].

Figure (2.14) shows a bootstrapped switch which is conceptually a single NMOS transistor. In the OFF state, the gate is grounded and the switch will be in the cutoff mode. In the ON state, a constant voltage of (V_{DD}) is applied across the gate-to-source terminals, and a low on resistance is formed from drain-to-source terminals independent of the input signal. If the gate voltage exceeds (V_{DD}) for a positive input signal, none of the terminal-to-terminal device voltages exceed (V_{DD}) [12].

Figure (2.15) shows the actual bootstrapped circuit. It operates on a single phase clock Ø that turns the bootstrapped switch M_{11}ON and OFF. When Ø is low, M_7 and M_{10} discharge the gate of M_{11} to ground and thus the bootstrapped circuit in the OFF phase. In this phase, (V_{DD}) is applied across capacitor C_3 by M_3 and M_{12}. This capacitor will act as a battery across the gate-to-source terminals of M_{11}during the ON phase. The job of M_8 and M_9 is to isolate the switch $M_{11}$from C_3 while it is charging. When Ø is high, the gate of M_8 will be pulled down by M_5, allowing charge from the battery capacitor C_3 to flow onto gate G. This turns on both M_9 and M_{11}. M_9 enables gate G to track the input voltage S shifted by (V_{DD}), keeping the gate-to-source voltage of M_{11} constant

regardless the input signal. For example, if the source S is at (V_{DD}), then gate G is at ($2V_{DD}$); however, ($V_{GS} = V_{DD}$). The body (n-well) of M_8 is connected to its source in order to repress latch up. M_7 and M_{13} are not functionally necessary but to improve the circuit reliability. M_7 reduces the (V_{DS}) and (V_{GD}) experienced by M_{10} when Ø is low. M_{13} ensures that (V_{GS8}) does not exceed (V_{DD}). M_1, M_2, C_1, and C_2 form a clock multiplier that enables M_3 to charge C_3 during the OFF phase [12].

C_3 must be sufficiently large to supply the stored charges to the gate-to-source terminals of M_{11}in addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to equation (2.7), where C_p is the total parasitic capacitance connected to the top plate of C_3 while it is across M_{11} [12]

$$V_G = V_S + \frac{C3}{C3+C_p} V_{DD} \tag{2.7}$$

When the bootstrapped switch is OFF, a C_{ds} capacitor is formed between the drain-to-source terminals of the sampling transistor. It couples the input signal to the sampling capacitor by C_{ds} and the routing parasitic capacitance. The coupling effect degrades the high frequency performance because C_{ds} induces unequal charges in the comparison cycles, which result in a dynamic offset. Therefore, two cross-coupled metal oxide metal (MOM) capacitors are used to neutralize the effect as shown in Figure (2.16). A dummy switch is an alternative solution to reduce the coupling effect [12,14].

As a result of using bootstrapped technique, the gate-to-source voltage of the sampling transistor will have a constant voltage and it is relatively independent of the input signal. This will improve the switch linearity and the input bandwidth [12].

A simulation was done for this circuit with the same input signal that is mentioned previously. Figure (2.17) shows the input clock pulses. The supply voltage (V_{DD}) is 1V and a clock pulses are formed on G that is shifted from the input signal by ($V_{DD} = 1V$) as shown in Figure (2.18). C_1, C_2, C_3, and C_s are chosen to be 0.5pF, 0.5pF, 10pF and 5pF respectively. Figure (2.19) shows zoomed ($V_{out,sampled}$) of this circuit with the clock formed on G. It has the same noise spectrum as the basic S/H circuit with total RMS output noise of 26.58 μV. The aspect ratios of the transistors are shown in Figure (2.15).

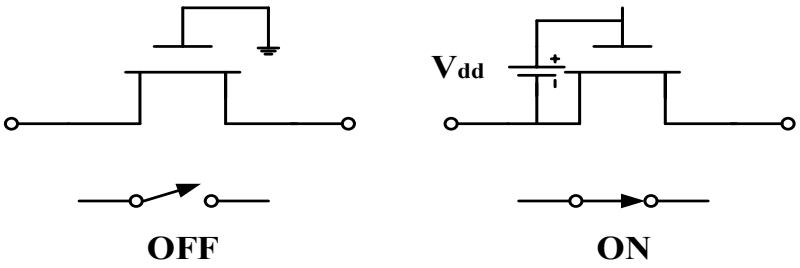


Figure 2.14 Bootstrapped MOS switch [12]

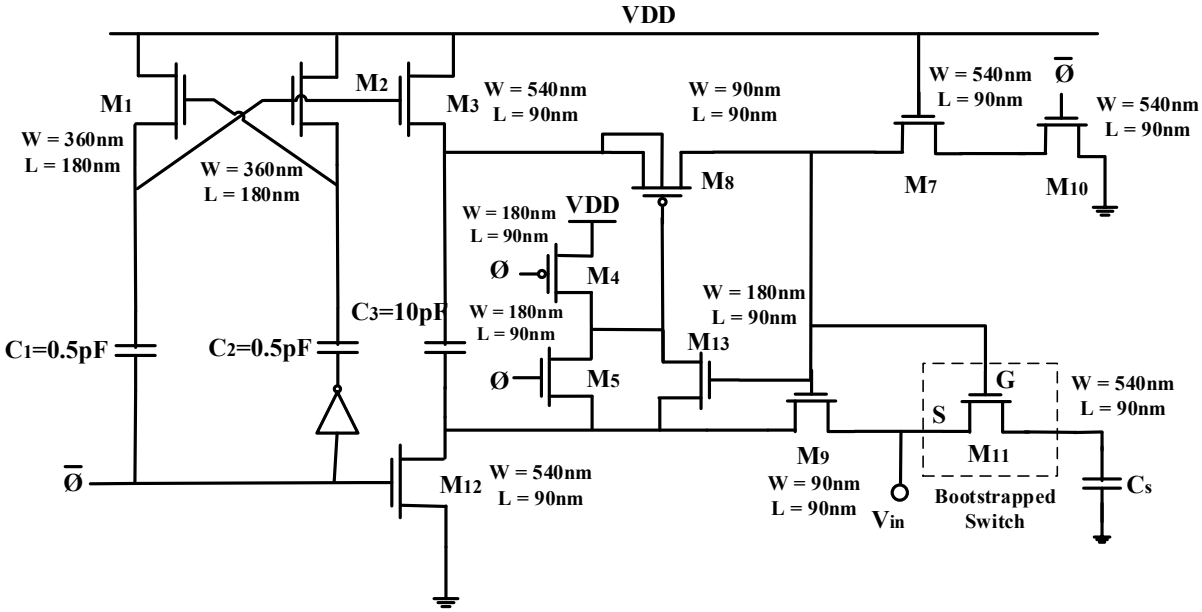


Figure 2.15 Sample and hold with bootstrapped circuit technique [12]

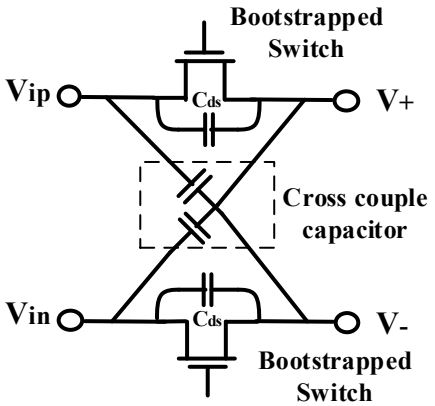


Figure 2.16 Cross-coupled capacitors [14]

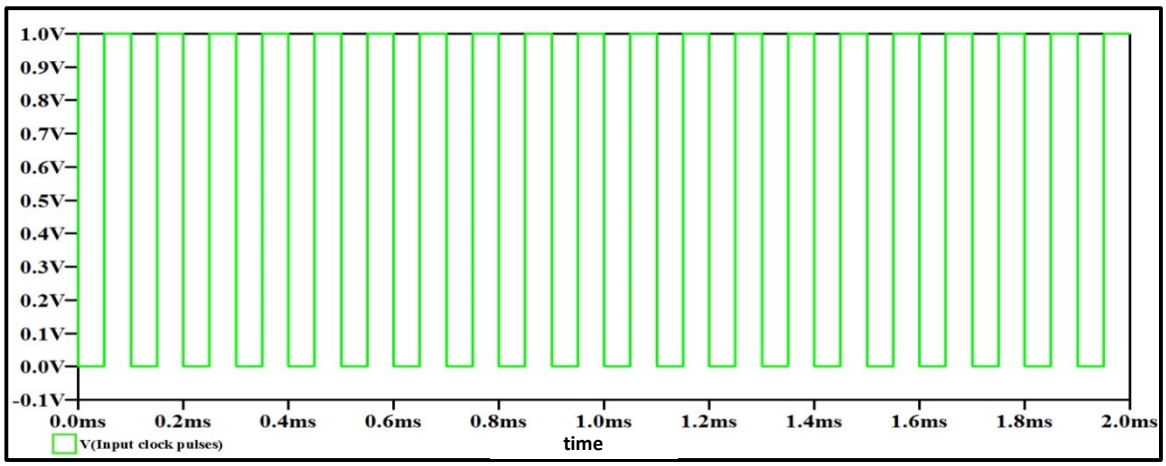


Figure 2.17 Input clock pulses (Ø)

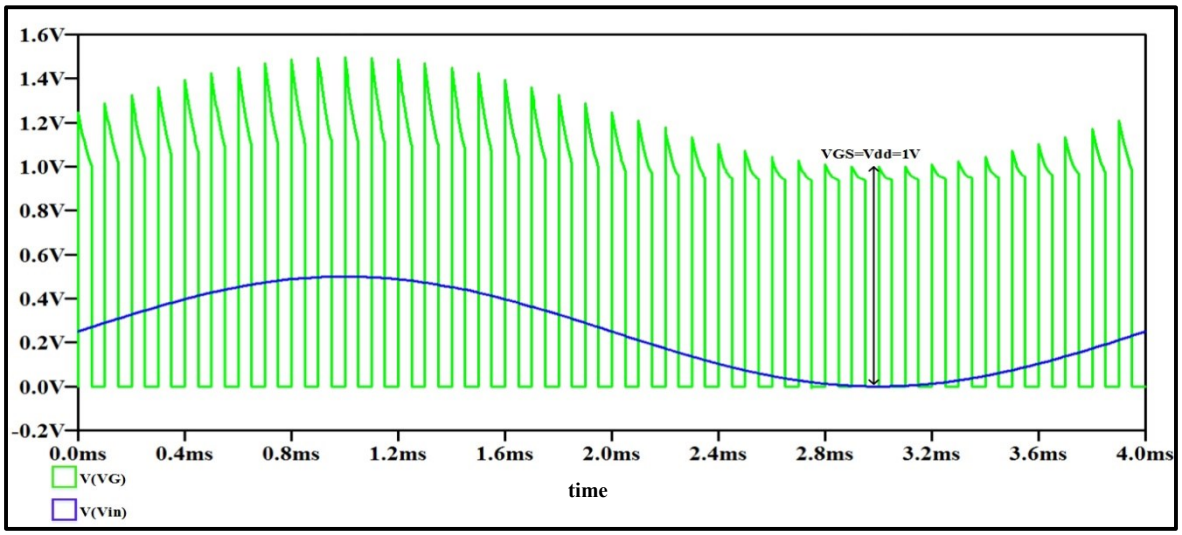


Figure 2.18 Input signal with the clock pulses formed on G

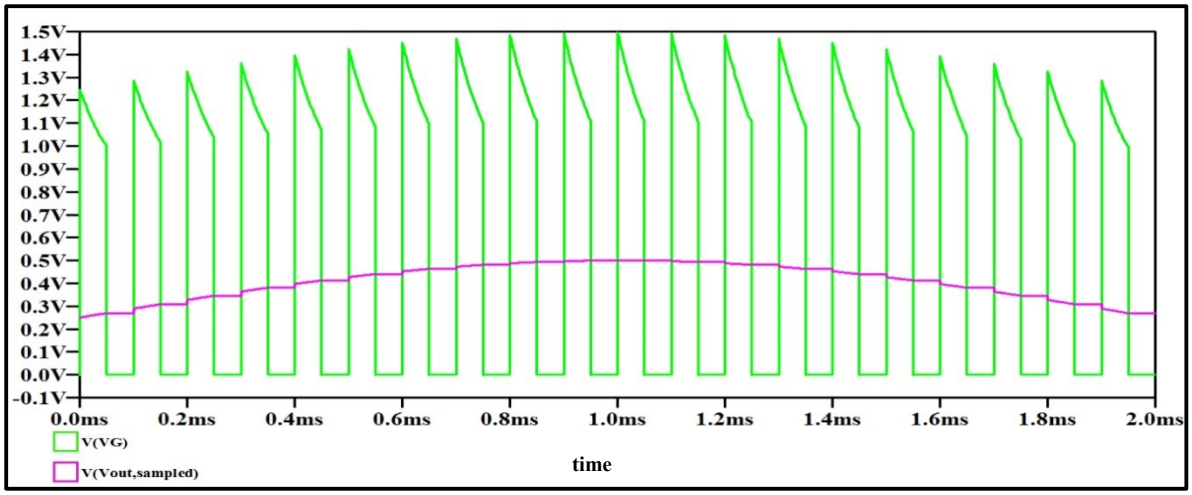


Figure 2.19 Zoomed ($V_{out,sampled}$) with the clock pulses formed on G

Finally, a power scalable technique of S/H circuit is introduced. Since the S/H circuit's working time frame is much smaller than the whole conversion period. It aims to save a large amount of static power when S/H circuit is idle during the conversion phase. So it becomes an essential circuit in high speed applications [15,16].

Figure (2.20) shows S/H circuit with power scalable ON/OFF technique. This technique can be added to any of the S/H circuits which were mentioned in this chapter. It is based on the addition of PMOS switch M_{p3} between the supply voltage and the output of the S/H circuit. When Ø is low (reset mode), the S/H circuit will be OFF. When Ø is high, M_{p3} is disconnected and the S/H circuit is in the ON mode. During the power down phase, M_{p3} will pull up the top plate of the sampling capacitor C_s which will degrade the speed during this phase. NMOS switch M_{N2} is consequently added between C_s and the ground in order to overcome this problem. So when Ø is low, C_s will be floating and the speed of the power down transient can be improved [16].

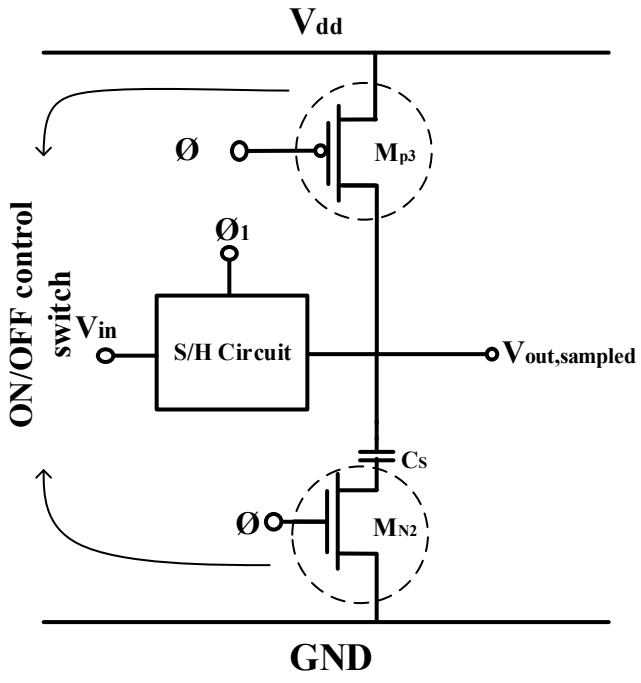


Figure 2.20 Sample and hold circuit with power scalable ON/OFF technique [16]

2.4 Proposed Modified Low-Power Bootstrapped Sample and Hold Circuit using Transmission Gate

A proposed modified low-power bootstrapped S/H circuit using transmission gate is illustrated in Figure (2.21). Simply, it is the same as the S/H circuit with bootstrapped technique which is shown in Figure (2.15) but without the multiplier circuit. The multiplier circuit consists of M_1, M_2, C_1 and C_2. In Figure (2.15), the gate of the NMOS transistor M_3, which is responsible for charging the capacitor C_3, is biased by the multiplier circuit. On the other hand, in Figure (2.21), the NMOS transistor M_3 is replaced by a PMOS transistor M_3 and its gate is biased by the gate of the bootstrapped switch M_{11}. M_3 will charge C_3 to (V_{DD}) in the OFF state of the bootstrapped switch M_{11}; while in the ON state, the stored charge in C_3 will be applied to the gate-to-source terminal of M_{11}. Both circuits make the gate-to-source voltage of M_{11} constant and equal to the supply voltage which is independent of the input signal. This result in small and constant on-resistance of the sampling switch. The main important feature of the proposed modified low-power bootstrapped S/H circuit using transmission gate is power consumption. It consumes less amount of power compared to the other two presented bootstrapped techniques in medium and high frequency applications. In addition to that, the SNDR will not have a degradation even in high frequency application when the input signal is 1 MHz or 7 MHz or 13.6 MHz. A simulation was done for this circuit with the same input signal that is mentioned previously and with the aspect ratios shown in Figure (2.21). It has the same noise spectrum as the basic S/H circuit with total RMS output noise of 26.59 uV.

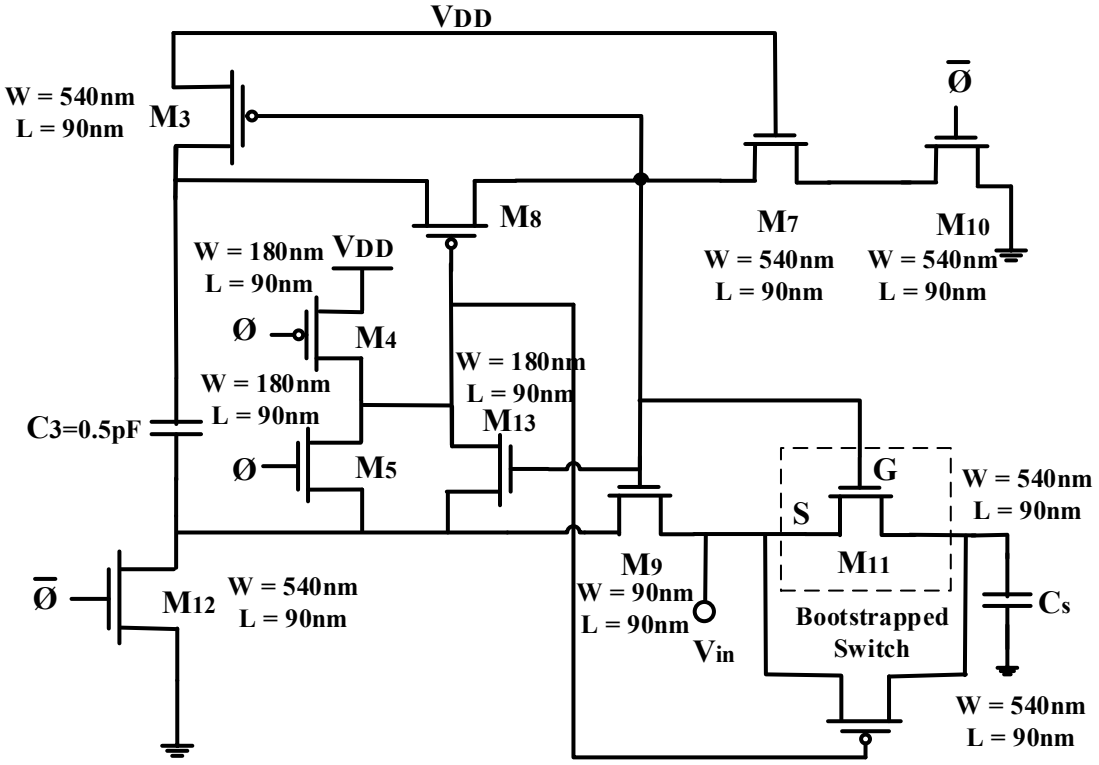


Figure 2.21 Proposed Modified low-power bootstrapped S/H circuit using transmission gate

2.5 Simulation Results

A simulation was done for the various introduced S/H circuits using 90nm CMOS technology on LT Spice IV. It is done on different applications from low (250 Hz), medium (10 KHz) to high (1 MHz, 7 MHz and 13.6 MHz) frequency. It is worth noting that the value of the sampling capacitor is a function of two main factors: the ADC input range and resolution, which translates into an equivalent thermal noise specification ($\frac{KT}{C_s}$) [2]. The sampling capacitor value was chosen based on the highest SNDR. It is chosen to be 5pf for low frequency application (ECG signal). While it is chosen to be 1pf for medium frequency application (audio signal). For high frequency applications (Bluetooth, DVB-H, and WLAN), the sampling capacitor C_s is 0.1pf.

Table (2.1) shows the simulation results of the presented S/H circuits for different applications for a 1V supply voltage and 500 mV_{p-p}. Signal to noise and distortion ratio (SNDR) was calculated for the different S/H using equation (2.8). It is calculated from the fast Fourier transform (FFT) spectrum by measuring the peak signal value and the distortions peak values over 45 cycles of ($V_{out,sampled}$). The output noise spectrum and the sampling rate were calculated over the interest bandwidth ($2BW_{signal}$). The average power consumption over one period is measured for the presented S/H circuits neglecting the required power to turn the switch ON and OFF. Figure (2.22) shows the FFT spectrum over 45 cycles of ($V_{out,sampled}$) for the basic S/H circuit. All the presented S/H circuits have the same FFT spectrum as the basic S/H circuit and the difference between them is illustrated in Table (2.1).

$$\text{SNDR (dB)} = 20\log\frac{\text{Signal Peak}}{\text{Distortions Peak+RMS Noise}} \quad (2.8)$$

As a result from this study, in term of high SNDR and low power consumption, the differential basic S/H circuit is the best candidate for low frequency applications, while S/H circuit with bootstrapped technique is the best candidate for medium to high frequency applications. In addition to that, all the presented S/H circuits' types have a closest value of SNDR in the low frequency application. This means that for low frequency signals, there is no significant effect of the presented S/H circuits on the SNDR value. Since the main objective of this work is to propose low power SA-ADC for portable biomedical applications. Therefore, it is focused on S/H circuits without active block and / or supply voltage which meets the requirements of biomedical (low-

frequency) applications and low power consumption. As a result, the basic S/H circuit with dummy switch was found the best candidate for single ended low power and high SNDR [17,18].

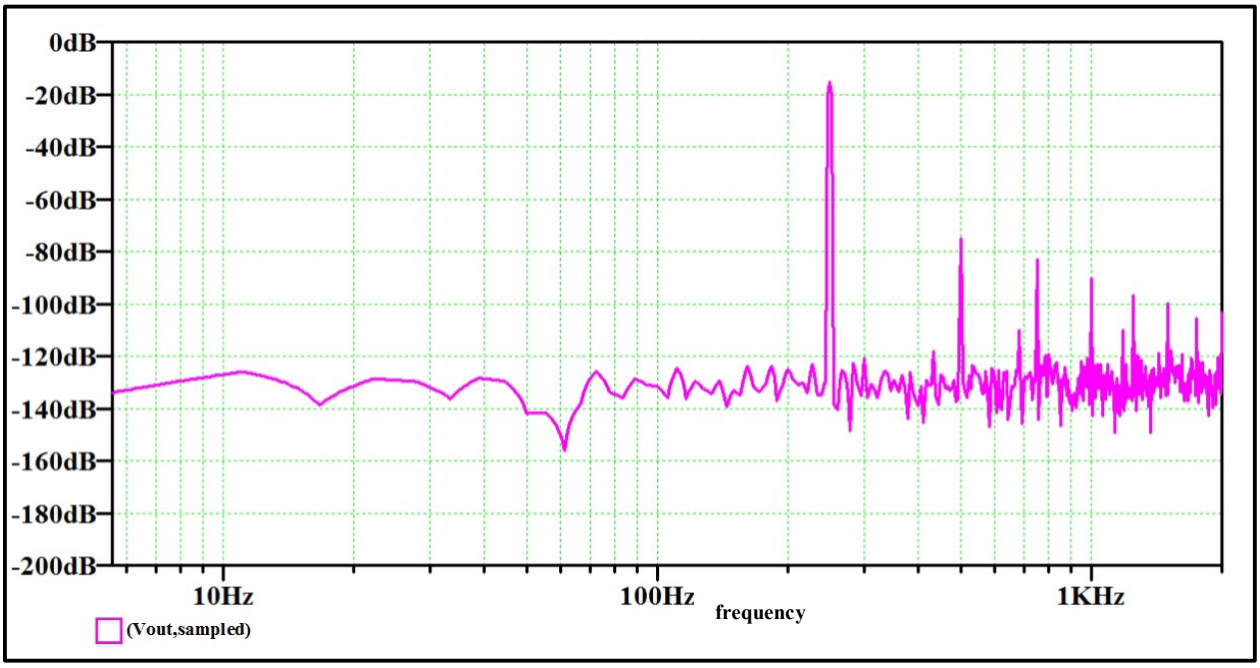


Figure 2.22 FFT spectrum of ($V_{out,sampled}$) for the basic S/H circuit

Table 2.1 Simulation results of the presented S/H circuits for different applications

S/H Type		Basic S/H	Differential Basic S/H	Basic S/H with Dummy Switch	Basic S/H with Transmission Gate	S/H with Boosted Driver Technique	S/H with Boot-strapped Technique	Proposed Modified Low-Power Bootstrapped S/H Circuit using Transmission Gate
Application	Parameters							
ECG 250 Hz	SNDR (dB)	54.34	56.27	54.39	54.42	54.65	54.63	54.66
	Average Power Consumption	-	-	-	1.4 pW	1.09 nW	29.82 nW	29.53 nW
	Sampling Rate	10 KS/sec						
	Total RMS Output Noise	26.58 µV	29 µV	26.57 µV	26.59 µV	26.59 µV	26.58 µV	26.59 µV
Audio 20 KHz	SNDR (dB)	53	32.6	53.01	53.7	65.27	65.13	65.14
	Average Power Consumption	-	-	-	3 pW	44.28 nW	51.64 nW	35.76 nW
	Sampling Rate	800 KS/sec						
	Total RMS Output Noise	70.13 µV	69.58 µV	70.09 µV	70.13 µV	70.13 µV	70.13 µV	70.13 µV
Bluetooth 1 MHz	SNDR (dB)	40.05	17.02	40.04	40.78	56.56	56.78	56.69
	Average Power Consumption	-	-	-	329.9 pW	2.06 µW	734.64 nW	201.09 nW
	Sampling Rate	40 MS/sec						
	Total RMS Output Noise	223.44 µV	223.07 µV	222.88 µV	223.17 µV	223.17 µV	223.44 µV	223.17 µV
DVB-H 7 MHz	SNDR (dB)	22.8	8.89	22.79	23.44	57.06	57	57.01
	Average Power Consumption	-	-	-	2.11 nW	12.68 µW	4.46 µW	883.57 nW
	Sampling Rate	280 MS/sec						
	Total RMS Output Noise	223.81 µV	223.07 µV	223.25 µV	223.55 µV	223.55 µV	223.81 µV	223.55 µV
WLAN 13.6 MHz	SNDR (dB)	17.41	6.44	17.40	17.73	56.75	56.71	56.706
	Average Power Consumption	-	-	-	3.22 nW	18.08 µW	8.38 µW	1.32 µW
	Sampling Rate	544 MS/sec						
	Total RMS Output Noise	223.84 µV	223.07 µV	223.28 µV	223.58 µV	223.58 µV	223.84 µV	223.58 µV

Chapter 3

Comparator Circuits

3.1 Introduction

The comparator is the second most widely used component in electronic circuits, after operational amplifier [3]. It is a key building block for applications where digital information needs to be recovered from analog signal especially in ADCs. It is the second block of the ADC components in which the output of S/H circuit seen by the input of the comparator. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system.

Figure (3.1a) shows the symbol of a differential comparator. Usually, the comparator stage is followed by a latch. Such comparators are well suited for logic circuits as the latch provides a large and fast output signal whose amplitude and waveform are independent of input signal. The transfer curve of the ideal differential comparator is illustrated in Figure (3.1b). In this Figure, the reference voltage (V_{ref}) is assigned to the negative input of the comparator. When the positive input is higher than (V_{ref}), then the output voltage is high (V_{OH}), and if it is lower than (V_{ref}), then the output is low (V_{OH}). The ideal transfer curve corresponds to an infinite differential gain. However, in the reality, the differential gain has a finite value which is (A_v). The transfer curve of such a comparator is shown in Figure (3.1c), where (V_{IL}) and (V_{IH}), are the input excess voltages called the overdrive. Overdrive is the input voltage that drive comparator from initial saturated input condition to a level required to switch the output state [3].

There are two types of comparators, static comparators, and dynamic comparators. In the static comparators, at every point in time (except during the switching transients), each gate output is connected to either (V_{DD}) or (V_{ss}) via a low-resistance path. It is used in medium speed applications. On the other hand, the dynamic comparators, relies on temporary storage of signal values on the capacitance of high impedance circuit nodes. It is used for high speed applications but it is more sensitive to noise [4]. It's worth noting that different sampling rates are used for different applications. This will affect the noise, speed and power consumption of the comparator

circuit and the overall ADC. Depending on the application, the emphasis will be on different metrics.

The objective of this chapter is to introduce various types of static and dynamic comparators in low voltage operation. All the presented comparators were analyzed, simulated and compared in term of complexity, dynamic range for proper operation regarding the mode of operation of the transistors, and average power consumption. The simulation was on LT Spice IV using 90nm CMOS technology under supply voltage of 1V. Furthermore, they were tested in low (250 Hz), medium (20 KHz), and high (1 MHz) frequency input signals in order to select the best comparator circuit candidate for the required application. This chapter is organized as follows: Section 3.2 illustrates static comparator circuits. Dynamic comparator circuits are presented in section 3.3. Each section includes its simulation results.

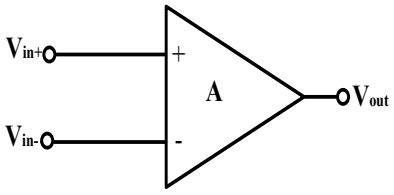


Figure 3.1a Differential comparator symbol [3]

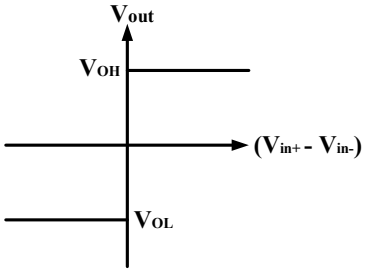


Figure 3.1b Transfer curve of ideal comparator [3]

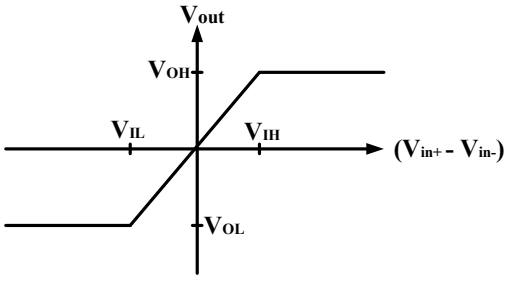


Figure 3.1c Transfer curve of real comparator with finite gain [3]

3.2 Static Comparators

Static comparator is a suitable choice for medium speed applications [2]. It has advantages of good performance and robustness (i.e. low sensitivity to noise), but unfortunately it has static power dissipation. The static power dissipation is due to the short circuit power dissipation which is the direct current path from the supply voltage to the ground while the switches are ON simultaneously for a short period [4].

Figure (3.2) shows the static comparator circuit with cross-coupled transistors. The circuit will execute the comparison between the inputs when the clock $\emptyset$ is low and both M_5 and M_6 transistors are turned OFF. If ($V_{in+} > V_{in-}$), the transistor M_2 will be ON, and the transistor M_1 is OFF. Therefore, (V_{out-}) is low, and M_3 turns ON causing (V_{out+}) high. On the other hand, if ($V_{in+} < V_{in-}$), the transistor M_2 will be OFF and the transistor M_1 will be ON. Therefore, (V_{out+}) is low and M_4 turns ON causing (V_{out-}) high. When the clock $\emptyset$ is high, the comparator circuit is operating in the resetting mode, and both outputs (V_{out+}) and (V_{out-}) are pulled high to (V_{DD}) via M_5 and M_6. The two inverters with a designated threshold voltage amplify the complimentary outputs to their full rail-to-rail logic levels. In the resetting phase, the comparator circuit is idle for a short time until the remaining blocks of the ADC complete their operation. The transistors M_5 and M_6 are included to avoid hysteresis or delayed response on the resetting phase which in turn speeds up the comparator. At node P, the dominant pole frequency of the comparator is located, and is given as follows:

$$\omega_p = \frac{g_{m1}}{C_p},\ C_p = C_{gs3} + C_{db2} + C_{db4} + C_{db\_6} + C_{buffer} \qquad (3.1)$$

Where C_p is the total capacitances at node P [2,11].

All the presented comparators in this chapter were simulated to evaluate their performance in low (250 Hz), medium (20 KHz) and high (1 MHz) frequency input signals for a sinusoidal wave with amplitude of 500 mV_{p-p}. In order to fit the 10 KS/s, 800 KS/s, and 40 MS/s sampling rate in low, medium, and high input frequency signals respectively of the 8-bit SA-ADC, the speed of the comparator must be operated at no less than 80 KHz, 6400 KHz, and 320 MHz respectively. For all the presented comparators; the supply voltage is 1V and the bias voltage is set to be 0.55V to generate low bias current. Figure (3.3) and Figure (3.4) shows the simulation of the static

comparator output and a zoomed part respectively. Table (3.1) and Table (3.2) shows the transistors' aspect ratios for (1 MHz) input frequency and the static comparator simulation results respectively. The transistors' aspect ratios for (250 Hz) and (20 KHz) input frequency are shown in Figure (3.2). All the introduced comparators have the same static comparator output shape and the main difference between them is illustrated in the simulation results Tables.

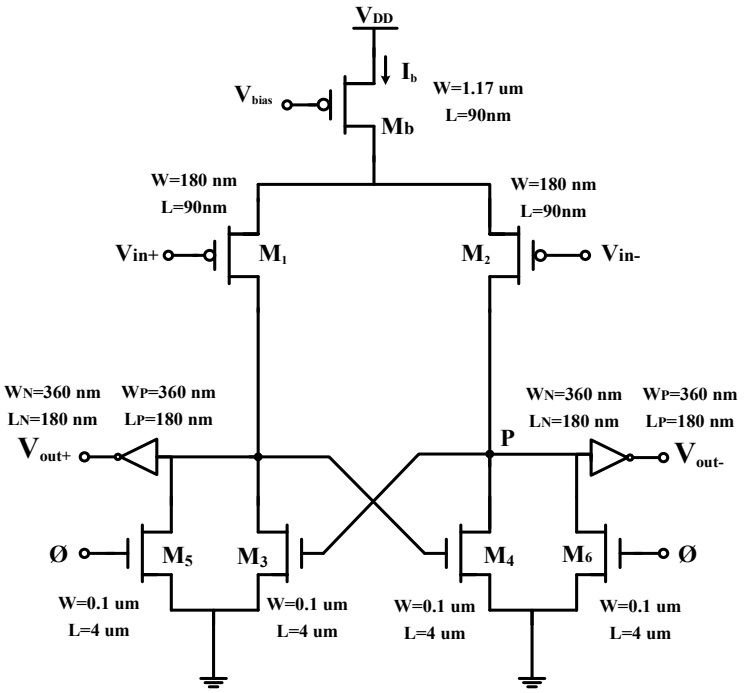


Figure 3.2 Static comparator with cross-coupled transistors [2]

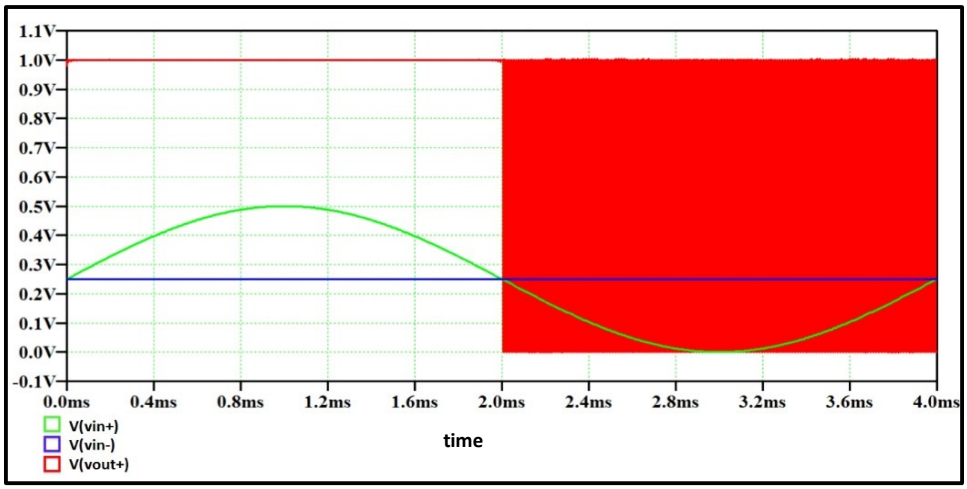


Figure 3.3 Static Comparator output when vin- = 0.25 V at speed of 80 KHz

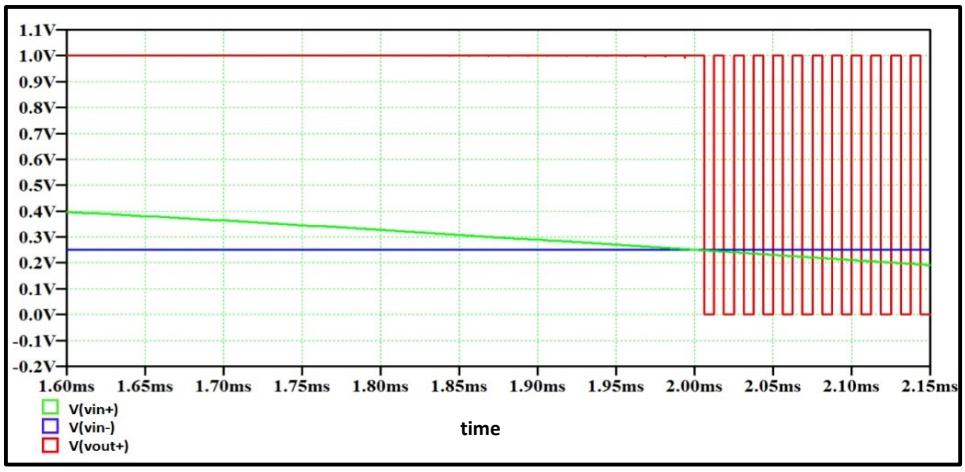


Figure 3.4 Zoomed static comparator output

Table 3.1 Transistors aspect ratios for static comparator with a cross-coupled transistors for high (1 MHz) input frequency signal

Transistor	Dimensions (W/L) (1 MHz)
M_1	540nm/180nm
M_2	540nm/180nm
M_3	0.1µm/180nm
M_4	0.1µm/180nm
M_5	0.1µm/180nm
M_6	0.1µm/180nm
M_b	1.17µm/180nm
inverters	360nm/180nm

Table 3.2 Static comparator simulation results for different applications

Frequency / Parameters		Low (250 Hz)	Medium (20 KHz)	High (1 MHz)
No. of transistors		11		
Dynamic Range of Vin- Based on the Dynamic Range of Vin+ (V)	Vin+ 0-0.5	0.01 – 0.5	0.01 – 0.5	0.04 – 0.49
	Vin+ 0.1-0.6	0.11 – 0.59	0.11 – 0.59	0.11 – 0.54
	Vin+ 0.2-0.7	0.21 – 0.69	0.21 – 0.65	0.22 – 0.56
Average Power Consumption	Vin+ 0-0.5 Vin- 0.25	637.68 nW	710.99 nW	1.84 µW
	Vin+ 0.1-0.6 Vin- 0.35	544.36 nW	626.68 nW	1.68 µW
	Vin+ 0.2-0.7 Vin- 0.45	429.9 nW	529.92 nW	1.43 µW

At low supply voltage, the maximum input signal swing of the ADC is limited which in turn leads to poor signal-to-noise ratio (SNR). In order to overcome such a problem, a rail-to-rail input range is required in the design. A comparator with a rail-to-rail common mode input range is necessary for this design in order to gain the required rail-to-rail input swing [11].

As shown in the Figure (3.5), the p- and n-type differential pairs are connected in parallel to extend the common mode input range to the power rails. These differential pairs eventually convert the differential input voltages into differential output currents. The summing up of currents drives the regenerative load formed by M_3 and M_4. Large differential output currents are produced by appropriate design of the tail currents of the differential pairs which drives the regenerative loads at worst conditions [11].

The major issue of using such a rail-to-rail comparator is that the offset of the comparator may depend on the common mode input. Consider (V_P) is the upper limit voltage such that the PMOS differential pair will not generate enough currents to trigger the regenerative load within a clock period once the common mode input is higher than it. Similarly, consider (V_N) is the lower limit voltage such that the NMOS differential pair will not affect the outputs of the comparator if the common mode input is below (V_N). Then the offset of the comparator will be dominated by the mismatch of the PMOS differential pair when the common mode input is between (V_{SS}) and (V_P). The NMOS differential pair and the current mirrors determine the offset if the common input is within the range from (V_N) to (V_{DD}). The offset of the comparator occurs due to the mismatch of both differential circuits between the two ranges discussed above which in turn results in distortion [11].

The two dominant factors that induce the input-referred offset voltage of a differential pair are the threshold voltage mismatch and the peripheral mismatch of the MOSFETs. The square standard deviation of the threshold voltage is known to be [11]:

$$\sigma^2 = (\Delta V_{th}) = \frac{A_{VT0}}{WL} \tag{3.2}$$

Where W and L is the effective channel width and length of the MOSFETs respectively, (A_{VT0}) is a process dependent constant. If both W and L are large enough, then the peripheral uncertainty is not a concern. Hence the area of the MOSFETs M_1, M_2, M_7, M_8 and M_9 to M_{12} were designed to be large in order to address the common mode input dependent offset [11].

Table (3.3) shows the simulation results of the static comparator with rail-to-rail input swing for low, medium, and high frequency input signals. Each transistor in the additional part in the rail-to-rail static comparator corresponds to each transistor in the static comparator has the same aspect ratio.

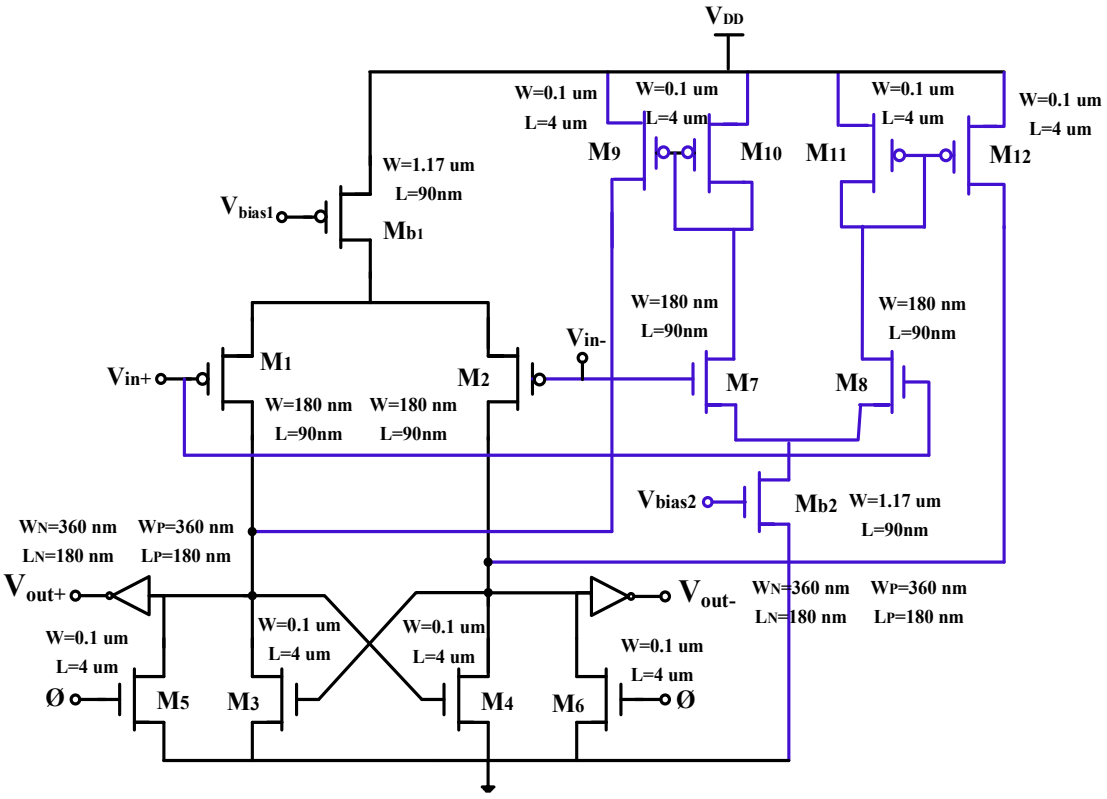


Figure 3.5 Static comparator with rail-to-rail input swing [11]

Table 3.3 Simulation results of rail-to-rail input swing static comparator for different applications

Frequency / Parameters		Low (250 Hz)	Medium (20 KHz)	High (1 MHz)
No. of transistors		18		
Dynamic Range of Vin- Based on the Dynamic Range of Vin+ (V)	Vin+ 0-0.5	0 – 0.5	0 – 0.5	0.04 – 0.46
	Vin+ 0.1-0.6	0.11 – 0.6	0.11 – 0.6	0.11 – 0.56
	Vin+ 0.2-0.7	0.2 – 0.7	0.21 – 0.7	0.21 – 0.64
Average Power Consumption	Vin+ 0-0.5 Vin- 0.25	1.27 µW	1.35 µW	3.203 µW
	Vin+ 0.1-0.6 Vin- 0.35	1.72 µW	1.82 µW	5.85 µW
	Vin+ 0.2-0.7 Vin- 0.45	2.31 µW	2.43 µW	10.08 µW

3.3 Dynamic Comparators

The trend of achieving both higher speed and lower power consumption in medium-to-high speed applications makes the dynamic comparators very attractive. It is also energy efficient design due to non-consumption of static current in contrast to the static comparator. This is done with the addition of a clock input which will block the current to flow between the supplies. However, the dynamic comparators are more sensitive to noise compared with the static comparator [4].

This section presents two types of dynamic comparators and some modifications which have the effect in improving its performance. Subsection 3.3.1 illustrate dynamic comparator with a cross-coupled transistors and a modified design of it. Dynamic latched comparator using back-to-back inverters, modified dynamic latched comparator and double-tail dynamic latched comparator are introduced in subsection 3.3.2.

3.3.1 Dynamic Comparator with a Cross-Coupled Transistors

Figure (3.6) illustrates the dynamic comparator schematic. The operational principle is as follows: When the clock $\emptyset$ is low, the comparator outputs (V_{out+}) and (V_{out-}) are reset high to (V_{DD}). When the clock $\emptyset$ goes high, the differential pair M_1 and M_2compares the two input voltages. According to the comparison result, the latch regeneration forces one output to be high and the other output to be low. The offset voltage of this comparator can be expressed as following:

$$V_{offset} = \Delta V_{th1,2} + \frac{(V_{GS}-V_{th})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right) \quad (3.3)$$

Where ($\Delta V_{th1,2}$) is the threshold voltage offset of the differential pair M_1 and M_2, $(V_{GS} - V_{th})_{1,2}$ is the effective voltage of the input pair, ($\Delta S_{1,2}$) is the physical dimension mismatch between M_1 and M_2, and (ΔR) is the loading resistance mismatch induced by M_{4P} to M_{7P}. The static offset is the first term which does not affect the performance of the ADC. However the signal dependent dynamic offset is the second term which degrades the performance of the ADC. The effective voltage of the input pair varies with the input common mode voltage [14]. Table (3.4) and Table (3.5) show the transistors' aspect ratios for (1 MHz) input frequency and the dynamic comparator with a cross-coupled transistors simulation results respectively. The aspect ratios for (250 Hz) and (20 KHz) input frequency are illustrated in Figure (3.6).

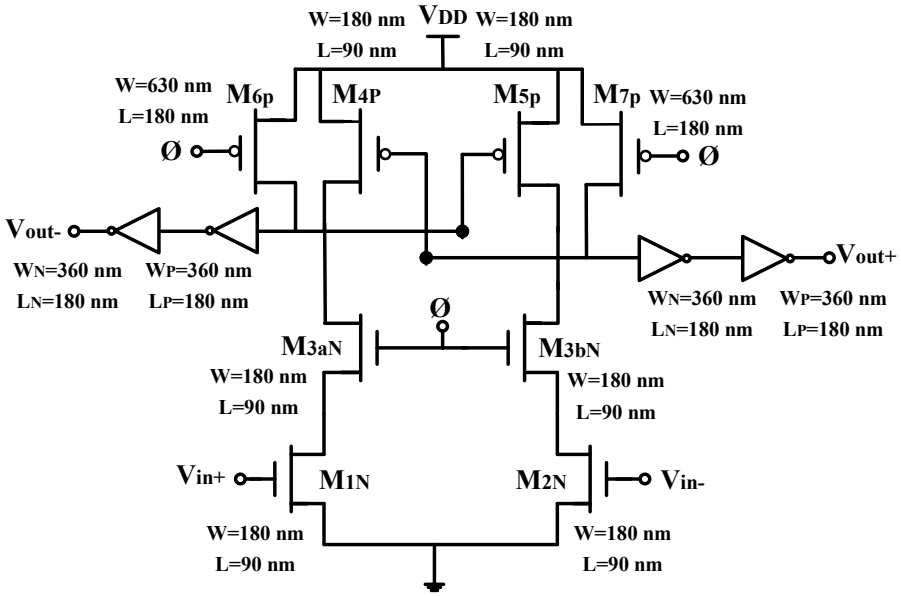


Figure 3.6 Dynamic comparator with a cross-coupled transistors [19]

Table 3.4 Transistors aspect ratios for dynamic comparator with a cross-coupled transistors for high (1 MHz) input frequency signal

Transistor	Dimensions (W/L) (1 MHz)
M_{1N}	4µm/1µm
M_{2N}	4µm/1µm
M_{3aN}	4µm/1µm
M_{3bN}	4µm/1µm
M_{4P}	180nm/90nm
M_{5P}	180nm/90nm
M_{6P}	4µm/1µm
M_{7P}	4µm/1µm
inverters	360nm/180nm

Table 3.5 Dynamic comparator with a cross-coupled transistors simulation results

Frequency / Parameters		Low (250 Hz)	Medium (20 KHz)	High (1 MHz)
No. of transistors		16		
Dynamic Range of Vin- Based on the Dynamic Range of Vin+ (V)	Vin+ 0-0.5	0.01 – 0.5	0.1 – 0.49	0.24 – 0.38
	Vin+ 0.1-0.6	0.12 – 0.52	0.11 – 0.52	0.24 – 0.4
	Vin+ 0.2-0.7	0.21 – 0.62	0.21 – 0.52	0.24 – 0.28
Average Power Consumption	Vin+ 0-0.5 Vin- 0.25	62 nW	187.71 nW	3.35 µW
	Vin+ 0.1-0.6 Vin- 0.35	148.44 nW	244.43 nW	9.17 µW
	Vin+ 0.2-0.7 Vin- 0.45	333.88 nW	450.81 nW	23.2 µW

There are many possible methods to improve the dynamic offset. The comparator size can be enlarged which results in larger power consumption. The effective voltage of the input pair can be reduced, but this decreases the comparison speed. A simple and reliable way is to insert a biased MOS $M_b$as shown in Figure (3.7). Figure (3.7) illustrates a dual circuit of the dynamic comparator in Figure (3.6) with a current source (biased MOS M_b) and a cross coupled NMOS transistors. Since $M_b$is in the saturation region, the change of its drain-to-source voltage has only a slight influence on the drain current. Hence $M_b$keeps the effective voltage of the input pair near a constant value when common mode voltage varies. Thus the dynamic offset has a minor influence on the conversion linearity. Therefore, this comparator circuit helps in avoiding the linearity degradation. Furthermore, during the conversion phase, the input voltages of the comparator reach to ground. The comparator uses a p-type input pair for proper functioning within the input common mode voltage range from half (V_{ref}) to ground [14]. This improved dynamic comparator diminishes the signal-dependent offset caused by the input common mode voltage variation. In addition to that, using a p-type input pair limit the noise bandwidth and minimize the ($^1/_f$) noise [20]. Table (3.6) and Table (3.7) show the transistors' aspect ratio for (1 MHz) input frequency and the simulation results of the modified dynamic comparator with a current source and a cross-coupled transistors respectively.

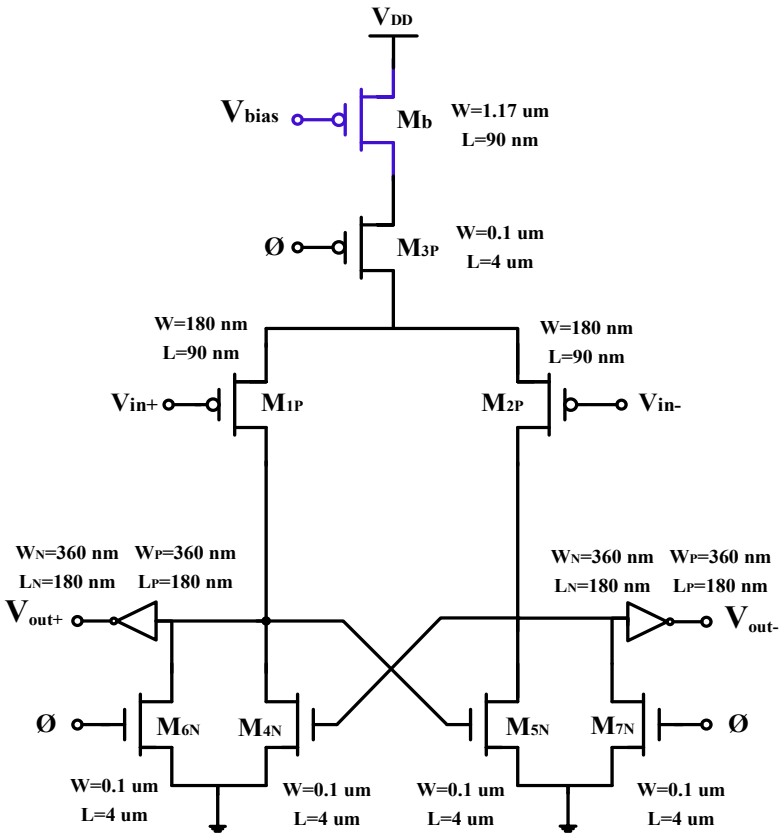


Figure 3.7 Modified dynamic comparator with a current source and a cross-coupled NMOS transistors [14]

Table 3.6 Transistors aspect ratios for a modified dynamic comparator with a current source and a cross-coupled NMOS transistors for high (1 MHz) input frequency signal

Transistor	Dimensions (W/L) (1 MHz)
M_{1p}	540nm/180nm
M_{2p}	540nm/180nm
M_{3P}	0.1µm/180nm
M_{4N}	0.1µm/180nm
M_{5N}	0.1µm/180nm
M_{6N}	0.1µm/180nm
M_{7N}	0.1µm/180nm
M_b	1.17µm/180nm
inverters	360nm/180nm

Table 3.7 Modified dynamic comparator with a current source and a cross-coupled NMOS transistors simulation results

Frequency / Parameters		Low (250 Hz)	Medium (20 KHz)	High (1 MHz)
No. of transistors		12		
Dynamic Range of Vin- Based on the Dynamic Range of Vin+ (V)	Vin+ 0-0.5	0 – 0.5	0.01 – 0.49	0.02 – 0.49
	Vin+ 0.1-0.6	0.1 – 0.59	0.1 – 0.59	0.11 – 0.52
	Vin+ 0.2-0.7	0.2 – 0.69	0.21 – 0.62	0.21 – 0.63
Average Power Consumption	Vin+ 0-0.5 Vin- 0.25	187.5 nW	238.26 nW	729.54 nW
	Vin+ 0.1-0.6 Vin- 0.35	138.01 nW	212.73 nW	656.1 nW
	Vin+ 0.2-0.7 Vin- 0.45	90.156 nW	198.97 nW	557.43 nW

3.3.2 Dynamic Latched Comparator using Back-to-Back inverters

Figure (3.8) illustrates a dynamic latched comparator using back-to-back inverters. This comparator consists of a pre-amplifier stage and a track and latch stage. The pre-amplifier stage is used to amplify the input signal and block the kickback noise. Although the output signal of the pre-amplifier is larger than the input signal, it is still not large enough to drive the digital circuit. A track and latch stage is needed to amplify the signal to logic by the positive feedback loop [21].

As shown in Figure (3.8), the differential pair $M_1$and M_2amplify the input signal and transistors M_5, M_6, M_7 and M_8 form a regeneration latch (two cross coupled NMOS and PMOS pairs which are stacked on top of each other). When the clock Ø is low, (V_{out+}) and (V_{out-}) are reset to (V_{DD}) via M_9 and M_{10}. When the clock Ø goes high, the differential pair $M_1$and M_2 compares the input (V_{in+}) and (V_{in-}) and a voltage difference is generated at the drain of transistors $M_5$and M_6.

This voltage difference is amplified by the positive feedback of the latch and (V_{out+}) and (V_{out-}) are goes to (V_{DD}) or ground according to the input voltages [21]. Table (3.8) illustrates the aspect ratios of the dynamic latched comparator using back-to-back inverters in the simulation for (20 KHz) and (1 MHz) input frequency. Table (3.9) shows simulation results of the dynamic latched comparator using back-to-back inverters. The aspect ratios for (250 Hz) input frequency are illustrated in Figure (3.8).

For more reliability and to avoid the effect of the comparison phase on the reset phase. An additional two PMOS transistors M_{P1} and M_{P2} with aspect ratio of (180nm/90nm) in low, medium, and high frequency input signals are added to the dynamic latched comparator as shown in Figure (3.9). Table (3.10) shows the simulation results for the modified latched comparator.

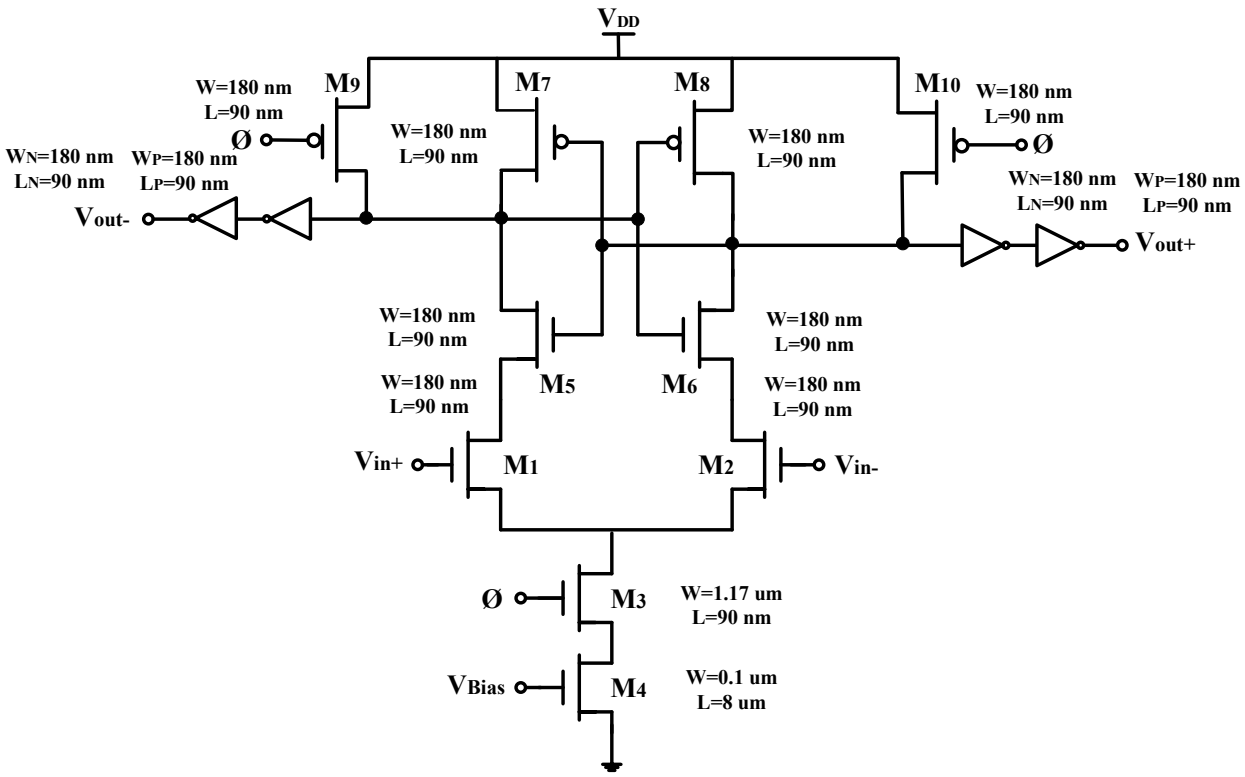


Figure 3.8 Dynamic latched comparator using back-to-back inverters [21]

Table 3.8 Transistors aspect ratios for dynamic latched comparator using back-to-back inverters for medium (20 KHz), and high (1 MHz) frequency input signals

Transistor	Dimensions (W/L) (20 KHz, 1 MHz)
M_1	4µm/1µm
M_2	4µm/1µm
M_3	1.17µm/1µm
M_4	8µm/90nm
M_5	180nm/90nm
M_6	180nm/90nm
M_7	180nm/90nm
M_8	180nm/90nm
M_9	180nm/90nm
M_{10}	180nm/90nm
inverters	360nm/180nm

Table 3.9 Dynamic latched comparator using back-to-back inverters simulation results

Frequency / Parameters		Low (250 Hz)	Medium (20 KHz)	High (1 MHz)
No. of transistors		18		
Dynamic Range of Vin- Based on the Dynamic Range of Vin+ (V)	Vin+ 0-0.5	0.01 – 0.48	0.12 – 0.49	0.21 – 0.47
	Vin+ 0.1-0.6	0.12 – 0.57	0.14 – 0.56	0.21 – 0.59
	Vin+ 0.2-0.7	0.21 – 0.69	0.21 – 0.69	0.22 – 0.7
Average Power Consumption	Vin+ 0-0.5 Vin- 0.25	15.89 nW	146.8 nW	1.24 µW
	Vin+ 0.1-0.6 Vin- 0.35	18.24 nW	196.66 nW	1.63 µW
	Vin+ 0.2-0.7 Vin- 0.45	22.46 nW	246.4 nW	2.16 µW

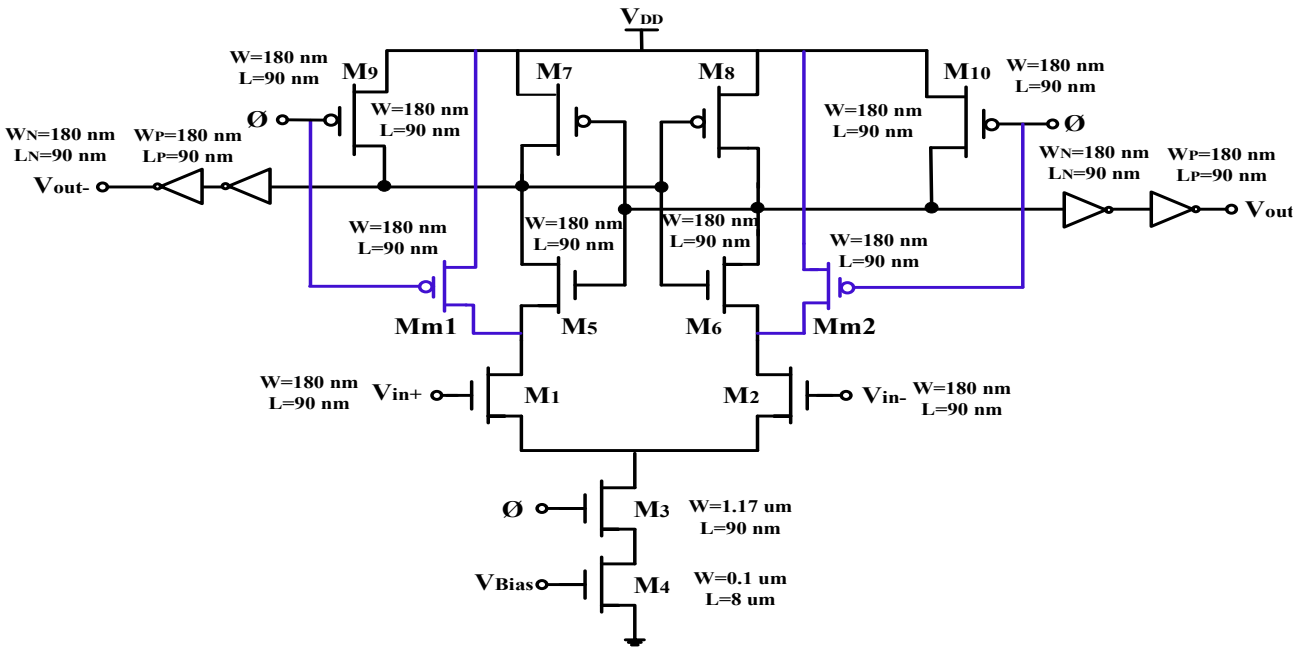


Figure 3.9 Modified dynamic latched comparator [22,23]

Table 3.10 Modified dynamic latched comparator simulation results

Frequency / Parameters		Low (250 Hz)	Medium (20 KHz)	High (1 MHz)
No. of transistors		20		
Dynamic Range of Vin- Based on the Dynamic Range of Vin+ (V)	Vin+ 0-0.5	0.01 – 0.49	0.13 – 0.44	0.22 – 0.49
	Vin+ 0.1-0.6	0.11 – 0.59	0.12 – 0.45	0.22 – 0.58
	Vin+ 0.2-0.7	0.22 – 0.68	0.21 – 0.58	0.22 – 0.69
Average Power Consumption	Vin+ 0-0.5 Vin- 0.25	16.55 nW	166.62 nW	1.302 µW
	Vin+ 0.1-0.6 Vin- 0.35	19.03 nW	221.35 nW	1.81 µW
	Vin+ 0.2-0.7 Vin- 0.45	23.15 nW	275.8 nW	2.39 µW

The advantages of this comparator is that, it achieves a fast decision due to strong positive feedback enabled by two cross-coupled pairs, and a low input referred offset enabled by the input differential pair stage. Furthermore, high input impedance, full swing output and no static power consumption. However, the stacking of transistors in this comparator requires quite a large voltage headroom, which becomes a problem as the supply voltage scaling in advanced CMOS technologies. Furthermore, due to the stacked PMOS and NMOS cross-coupled pairs with the input pair, the current flowing through these cross-coupled pairs is limited by the input common mode voltage of the differential pair. As a result, the speed and offset of the comparator depend on the input common mode voltage, which will slow down the comparison. This will be a problem for applications requiring a wide common mode range in A/D converters [22].

A double tail dynamic latched comparator is introduced in order to overcome the dynamic and the modified dynamic latched comparator problems. It uses one tail for the input stage and other for the latching stage as shown in Figure (3.10). This configuration has less stacking and therefore can operate at lower supply voltages.The double tail enables large current for fast latching independent of the common mode voltage at the latching stage and a small current for low offset and noise at the input stage [22].

The signal behaviour also shown in Figure (3.10). During the reset phase ($\emptyset = 0$), transistors M_9 and M_{10} precharge the gate of M_{11} and M_{12} to (V_{DD}). Accordingly V_{out+} and V_{out-} will be high. After the reset phase, the tail transistors M_3 and M_{13} turned ON ($\emptyset = V_{DD}$). At the drains of the differrential pair nodes, the common mode voltage drops monotonically with a rate defined by $(\frac{I_{M3}}{C_{\text{differential pair drains}}})$ and on top of this, an input dependednt differential voltage (ΔV_{Di}) will build up. The intermediate stage formed by M_{11} and M_{12} passes (ΔV_{Di}) to the cross coupled inverters and also provides additional shielding between the input and output which results in less kickback noise. As soon as the common mode voltage at the drains of the differential pair nodes is not enough for $M_{11}$and M_{12} to clamp its drain to ground, the inverters starts to regenerate the voltage difference. The ideal operating point (V_{CM}) and the timing of various phases can be tuned with the transistor sizes. As a result, the advantages of the double tail topology, it has better optimization of the balance between speed and offset independently, power and common mode voltage. In addition to that, it has a better isolation between the input and output of the comparator which results in less kickback noise and is well suited to operate under low supply voltages with low

power consumption [22]. Table (3.11) shows the double-tail dynamic latched comparator simulation results. The transistors' aspect ratios for (250 Hz), (20 KHz) and (1 MHz) input frequency are illustrated in Figure (3.10).

This work is focused on proposing low power SA-ADC for portable biomedical applications. Therefore, as a result the comparison which done for the mentioned comparator circuits. The double-tail dynamic latched comparator achieves the requirements of low power consumption, medium speed and proper dynamic range for low frequency applications comparing with the other mentioned comparator circuits. This is achieved due to the double tail and less stacking structure.

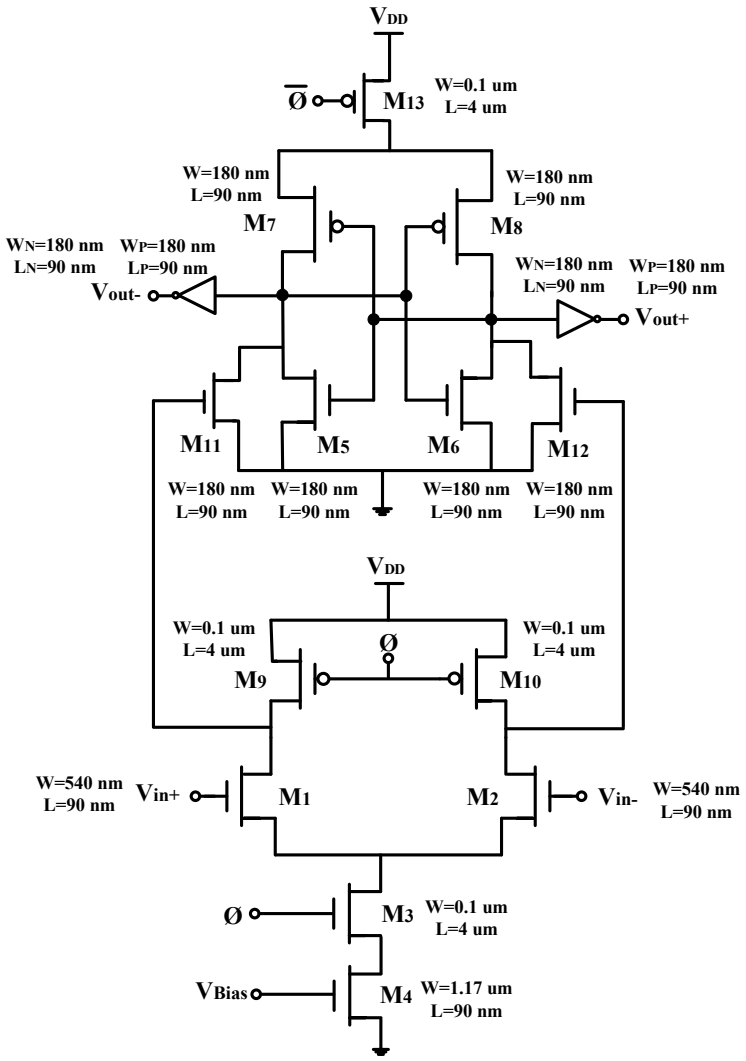


Figure 3.10 Double tail dynamic latched comparator [22]

Table 3.11 Double-tail dynamic latched comparator simulation results

Frequency / Parameters		Low (250 Hz)	Medium (20 KHz)	High (1 MHz)
No. of transistors		13		
Dynamic Range of Vin- Based on the Dynamic Range of Vin+ (V)	Vin+ 0-0.5	0.11 – 0.49	0.13 – 0.49	0 – 0.49
	Vin+ 0.1-0.6	0.13 – 0.59	0.17 – 0.59	0.1 – 0.6
	Vin+ 0.2-0.7	0.21 – 0.7	0.21 – 0.69	0.2 – 0.7
Power Consumption	Vin+ 0-0.5 Vin- 0.25	12.27 nW	97.6 nW	651.24 nW
	Vin+ 0.1-0.6 Vin- 0.35	12.23 nW	94.07 nW	644.29 nW
	Vin+ 0.2-0.7 Vin- 0.45	12.26 nW	97.18 nW	642.86 nW

Chapter 4

Digital-to-Analog Converter

4.1 Introduction

There are four main types of digital-to-analog converter (DAC) circuits which are decoder based, binary weighted, thermometer code and hybrid [3]. The main theme of this work is to reduce the power consumption therefore, the binary weighted DAC is the most suitable type in term of low power [2]. The binary weighted type might be binary arrays of currents signals (in resistor or current approaches) or binary weighted arrays of charges [3]. The conventional voltage driven R-2R techniques suffers from difficulties in the fabrication process. In addition to that, it requires careful control of the on-resistance ratios in the MOS switches over a wide range of values. Therefore, the binary weighted arrays of charges is preferred due to the following advantages: As the MOS device is used as a charge switch, it has inherently zero offset voltage and as an amplifier, it has very high input resistance. In addition to that, capacitors are easily fabricated in metal gate technology. As a result, using the capacitors rather than the resistors as the precision components, and using the charge rather than the current as the working medium [24].

The objective of this chapter is to study several DAC topologies in order to reduce the switching energy in the capacitance for low power applications. However the suitable topology will be selected. A simulation was done for the selected DAC topology on LT Spice IV using 90nm CMOS technology in low voltage operation (reference voltage is 1V). This chapter is organized as follows: Section 4.2 illustrates binary weighted switched capacitor array DAC. Serial charge redistribution DAC is presented in section 4.3. Section 4.4 described junction-splitting capacitor array DAC and the simulation results are illustrated in section 4.5.

4.2 Binary Weighted Switched Capacitor Array DAC

Figure (4.1) shows a schematic diagram of an 8-bit binary weighted switched capacitor array DAC which consists of nine switches from S_0 to S_8. S_0 is implemented using an NMOS switch. S_1 to S_8 are implemented using an NMOS and PMOS switches and these switches are controlled by the successive approximation register (SAR) controller. Each capacitor in the binary weighted array has a value of [6,11].

$$C_i = 2^{i-1}C_0 \text{ where } i=\{1,2,\ldots 8\} \quad (4.1)$$

Where C_0 is the value of the unit capacitor in the DAC. The power source of these passive capacitor array is the reference voltage (V_{ref}). By calculating the required charge of all the capacitors during charging and discharging periods, the power consumption of (V_{ref}) supply when the input voltage V_{in} is applied can be analyzed and it is [11,25].

$$P_{Vref}(V_{in}) = \left(\frac{V_{ref}}{T}\right)\sum_{i=1}^{9} Qc_i \quad (4.2)$$

Where T is the period in which the DAC take it to convert a sample and Qc_i is the total charge supplied by (V_{ref}) during the i^{th} cycle to the DAC. The operation of the binary weighted switched capacitor array can be summarized as follows [11]:

- In the first cycle, all the capacitors are connected to ground, so the total charge supplied by V_{ref} is zero.
- In the second cycle the most significant bit (MSB) switch S_8 is switched to (V_{ref}) while the other capacitor are kept connected to ground, then the output voltage of the DAC is:

  $$V_{DAC8} = V_{ref}\frac{C_8}{C_{total}} \quad (4.3)$$

  Where C_{total} is the total capacitance of the DAC and the charge supplied by (V_{ref}) in the second cycle can be calculated:

  $$Qc_2 = C_8[(V_{ref} - V_{DAC8}) - (0 - 0)] \quad (4.4)$$

  If $V_{DAC8} > V_{in}$, Q_8 is 1 and S_8will be kept connected to (V_{ref}), otherwise Q_8 is 0 and S_8will be switched to ground.
- In the third cycle, S_7 will be switched to (V_{ref}) and the output voltage of the DAC is:

$$V_{DAC7} = V_{ref} \frac{C_7 + Q_8 C_8}{C_{total}} \quad (4.5)$$

In case of $Q_8 = 1$, then the charge that stored in C_8 in the second cycle will be shared with C_7 in the third cycle, so the charge provided by (V_{ref}) in the third cycle is:

$$Qc_3 = C_7[(V_{ref} - V_{DAC7}) - (0 - V_{DAC8})] + Q_8 C_8[(V_{ref} - V_{DAC7}) - (V_{ref} - V_{DAC8})]$$

$$= C_7(V_{ref} - V_{DAC7} - V_{DAC8}) + Q_8 C_8(V_{DAC8} - V_{DAC7}) \quad (4.6)$$

- The operation is continued for the remaining switches in the same technique, the output voltage and the charge can be calculated in each cycle in the same way by using the general expression for each. The general expression for Qc_i is:

$$Qc_i = C_{10-i}\left[\left(V_{ref} - V_{DAC(10-i)} + V_{DAC(11-i)}\right)\right] +$$

$$\sum_{j=11-i}^{8} Q_j C_j \left(V_{DAC(11-i)} - V_{DAC(10-i)}\right), i \in \{3,..,9\} \quad (4.7)$$

and the general expression for (V_{DACi}) is:

$$V_{DACi} = V_{ref} \frac{C_i + \sum_{j=i+1}^{8} Q_j C_j}{C_{total}} \quad (4.8)$$

Where $i = \{0,..,7\}$ and it is the number of the capacitor switched to (V_{ref}) in each cycle and C_{total} is the total capacitance of the DAC.

- The power consumed by the reference voltage can be estimated using the below equation.

$$P_{Vref}(V_{in}) = \frac{f_{clk}}{9} 2^8 C_0 \left(\frac{5}{6} V_{DD}^2 - \frac{1}{2} V_{in}^2\right) \quad (4.9)$$

Where f_{clk} is the sampling frequency of the DAC. Smaller capacitor of C_0 of 50 fF can save the power consumption. However, it will also contribute to an increase in thermal noise (it is an electronic noise due to the thermal agitation of the charge carrier regardless of any applied voltage and when it is related to a capacitor it is also called a KTC noise) which degrade the resolution of the DAC [6,11].

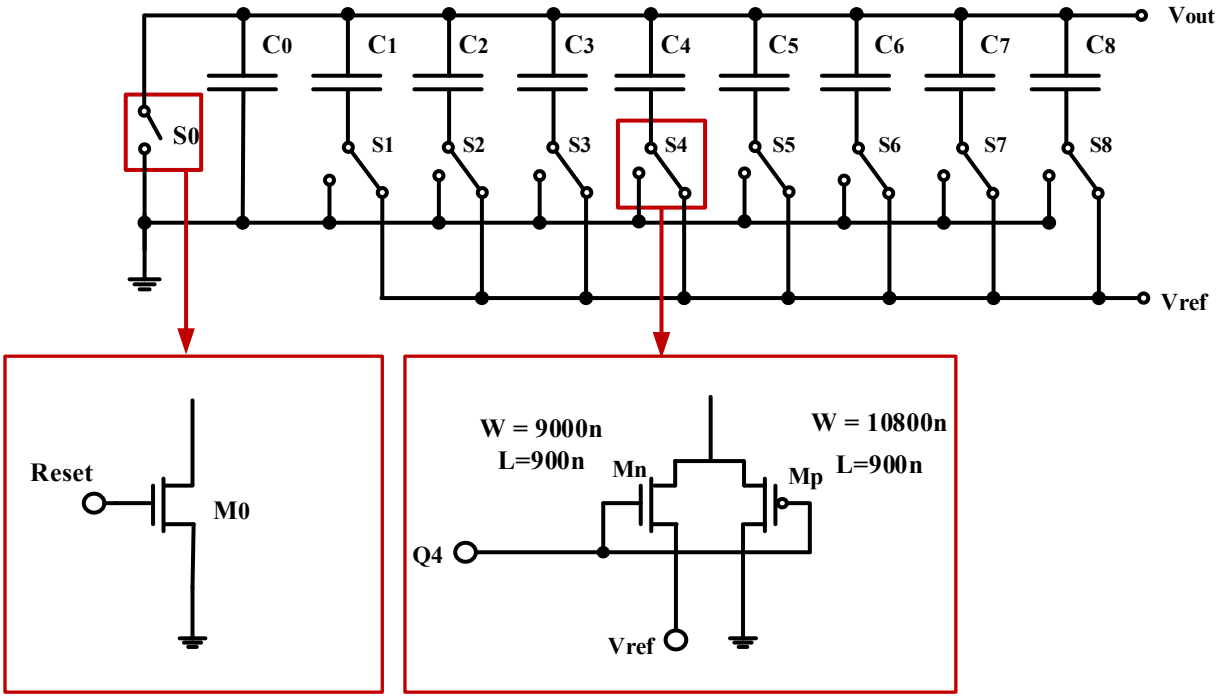


Figure 4.1 Schematic diagram of binary weighted switched capacitor array DAC [2,11]

4.2 Serial Charge Redistribution D/A Converter

A simplified schematic diagram of a serial charge redistribution DAC circuit is shown in Figure (4.2). Capacitors C_1 and C_2 are nominally of equal value. Conversion is accomplished serially by considering the least significant bit (LSB) Q_0 first. Capacitor C_1 is pre-charged either to the reference voltage (V_{ref}) by a momentary closure of S_2 if $Q_0 = 1$ or to ground through S_3 if $Q_0 = 0$. Simultaneously, C_2 is discharged to ground through S_4. With S_2, S_3, and S_4 open, switch S_1 is then closed momentarily to redistribute the charge, and the resulting capacitor voltages are [25]:

$$V_1(1) = V_2(1) = \frac{Q_0}{2} V_{ref} \quad (4.10)$$

Holding the charge on C_2, the pre-charging of C_1 is repeated, this time considering the next LSB Q_1. After redistribution the capacitor voltages are [25]:

$$V_1(2) = V_2(2) = \frac{1}{2}(Q_1 + \frac{Q_0}{2})V_{ref} \quad (4.11)$$

The process continues in this fashion, and at the end of n-redistribution, the existing charge on C_2 is divided by two and a charge increment corresponding to $\frac{Q_n}{2} V_{ref}$. Therefore, for an n-bit DAC, the voltage on the capacitor is [25]:

$$V_1(n) = V_2(n) = \sum_{i=1}^{n} \frac{2^i Q_i}{2^{n+1}} V_{ref} \quad (4.12)$$

Which is the desired output. A total of n-pre-charge steps and n-redistributions are required to complete an n-bit D/A conversion. Table (4.1) illustrates the operation of the serial charge redistribution DAC [25].

The advantage of serial redistribution DAC is reducing the switching energy since just two basic capacitors are required to be charged. However for an n-bit conversion, **n(n+1)** charging steps are required which result in decreasing the sampling frequency. In the case of an 8-bit SAR ADC, 72 clock cycles are required per each conversion, half for charging and half for the redistribution [25].

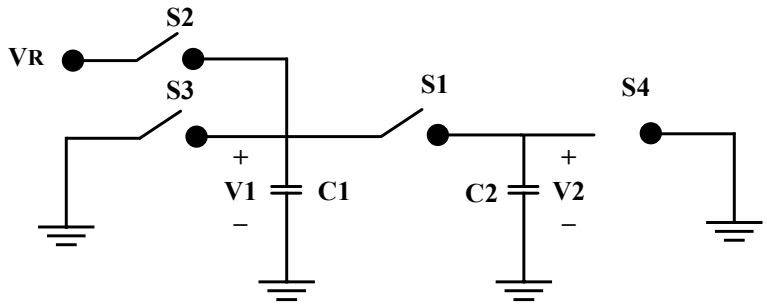


Figure 4.2 Schematic diagram of serial charge redistribution DAC [25]

Table 4.1 Serial charge redistribution DAC operation [25]

Cycle No.	DAC Input Bits						Comparator Output	No. of Charging Steps
	Q_1	Q_2	Q_3	…	Q_{n-1}	Q_n		
1	1	-	-	…	-	-	a_n	2
2	1	a_n	-	…	-	-	a_{n-1}	4
3	1	a_{n-1}	a_n	…	-	-	a_{n-2}	6
…	…	…	…	…	…	…	…	…
n	1	a_2	a_3	…	a_{n-1}	a_n		2n
TOTAL								n(n+1)

4.3 Junction-Splitting Capacitor Array

The junction-splitting (J-S) capacitor array consists of a number of serially connected sections each of which is composed of splitting capacitor as shown in Figure (4.3). Each section represents sub-capacitor section which is also shown Figure (4.3). The number in each section is the total capacitance of the sub-capacitor section. This capacitor array has an additional switches to connect the top plates of the sub-capacitor sections serially, thus it is called junction-splitting (J-S) capacitor array [26].

The conventional binary weighted switched capacitor array DAC creates the desired output voltage by re-arranging the switches for a cycle which causes energy waste. However in J-S capacitor array, the desired output voltage is created by joining a sub-capacitor section to the previous capacitor array. That means C_{tot} is not constant and it increases during the conversion process [26].

Figure (4.4) shows the method of achieving the desired capacitor ratio for the J-S capacitor array. C_{tot} and C_H represent the denominator and numerator respectively. First the MSB Q_0 is determined by comparing the input voltage with half reference voltage. The half reference voltage is achieved by connecting one of the smallest capacitors to the ground and the other connected to the reference voltage. Then, the next output voltage will be achieved by connecting a sub-capacitor section one at a time. The total capacitance of a sub-capacitor section to be added to the denominator and, $C_{\Delta tot}$ is the same as that of the present total capacitance. The capacitance to be added to the numerator is $C_{\Delta H}$ which determined by the results of previous comparisons $\{Q_i\}$ [26].

In general, $C_{\Delta H}$ to be added at step i (i>0) is determined by C $(2^{i-1}Q_0+2^{i-2}Q_1+2^{i-3}Q_2+\ldots\ldots\ldots+2^{i}Q_{i-2}+2Q_{i-1})$ where C is a unit capacitance. In step 0, $C_{tot} = 2C$, and $C_H = C$. Hence the i^{th} sub capacitor section consists of i capacitors as shown in Figure (4.3), where n_j means the node controlled by the j^{th} bit. The total capacitance of the i^{th} section is 2^iC which is equal to the sum of capacitance of all previous sections at right side. In a section, each capacitor has two switches which are controlled by one of the previously determined bits. A capacitor is connected to ground through a switch denoted by S_j^o if the corresponding bit Q_j is 0, otherwise it is connected to the reference voltage through a switch S_j^1 [26].

As shown in Figure (4.3), a capacitor in each section has a pair of switches. Each section is connected to the remaining sections via switches since all the capacitors are controlled by the same bit which connected through a pair of switches. Therefore, each section has only one pair of switches. For n bit digital outputs, the J-S capacitor array structure has 3n+2 switches, due to the n sections including the 0^{th} section in which each of them requires a pair of switches and one switch for the two adjacent sections which connected serially as shown in Figure (4.3). In this topology, the simulation results obtained in [26] show that the J-S capacitor array reduce the average energy consumed in the capacitor array by 75% and 60% compared to the conventional method and the splitting capacitor method reported in [27], respectively.

On the other hand, there are several drawbacks with this topology. The main problem comes from floating switches and floating capacitors are needed in this topology and therefore, the parasitic capacitance on the top plate and the one on the bottom plate are not equal which affect the SA-ADC linearity.

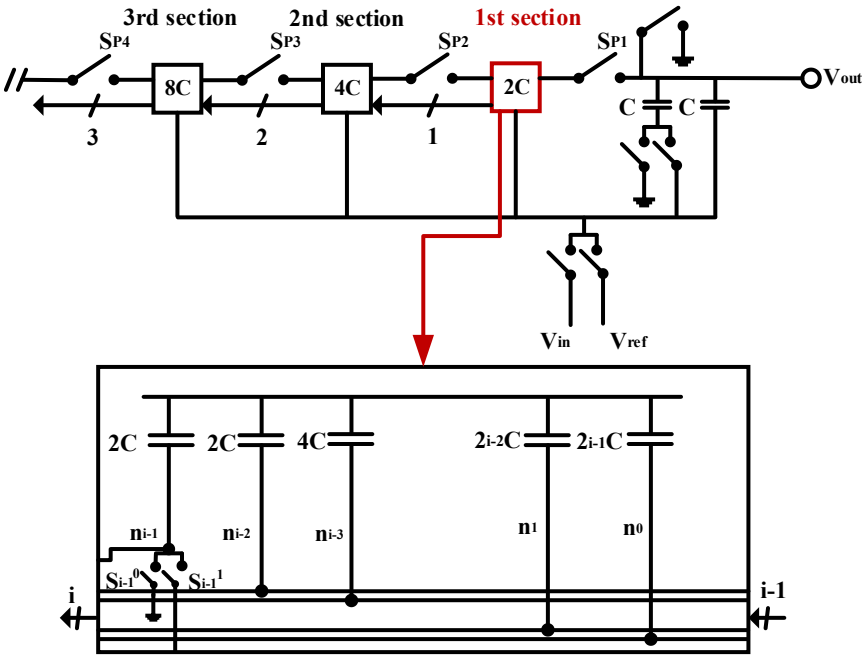


Figure 4.3 Junction splitting capacitor array DAC [26]

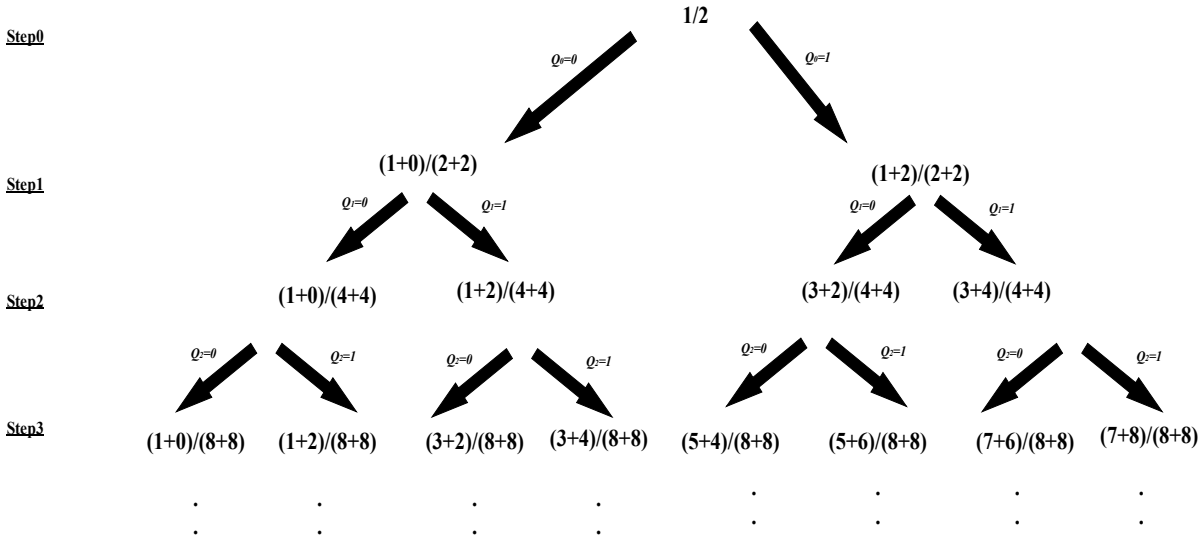


Figure 4.4 Method of achieving the desired capacitor ratio for the J-S capacitor array [26]

4.4 Simulation Results

Although the J-S capacitor array reduce the switching energy, it has disadvantage of the floating switches which results in parasitic capacitances which affect the SA-ADC linearity. Furthermore, the advantage of serial redistribution DAC is reducing the switching energy. However for an n-bit conversion, **n(n+1)** charging steps are required. This result in decreasing the sampling frequency. In the case of an 8-bit SAR ADC, 72 clock cycles per each conversion, half for charging and half for the redistribution. Hence, the traditional binary weighted capacitor array DAC has been chosen for low power approach in low frequency applications [2]. Another justification will be mentioned in Chapter 6 for choosing the traditional binary weighted capacitor array DAC.

A simulation was done for the traditional binary weighted capacitor array DAC using 90nm CMOS technology on LT Spice IV. It is worth noting that the value of the unit capacitor is a function of two main factors: the ADC input range and resolution, which translates into an equivalent thermal noise specification (KT/C). The unit capacitor value was chosen to trade off

the design between power consumption and noise contribution. Moreover, the matching and noise in the capacitor array will dominate the accuracy of the DAC. However, the process variation resulting in matching error commonly plays a more important role compared with the thermal noise. Hence, the unit capacitor is chosen to be 50fF. The layout of the capacitor array based on the N-select layer, active layer, capacitor ID, poly silicon and metal 1 using the L-Edit simulator. Table (4.2) shows the calculated value, measured value, and the percentage error of set of digital inputs. Figure (4.5) illustrates the DAC output voltage for (1000 0000) digital input. The aspect ratios are illustrated in Figure (4.1). The reference voltage is 1V.

Table 4.2 Binary weighted switched capacitor array DAC simulation results

Digital Input	Calculated Value (V)	Measured Value (V)	Percentage Error (%)
0000 0000	0	0	0
1000 0000	0.5	0.5	0
1000 1000	0.53	0.53	0
1100 1100	0.79	0.76	3.7
1111 1111	0.99	0.96	3

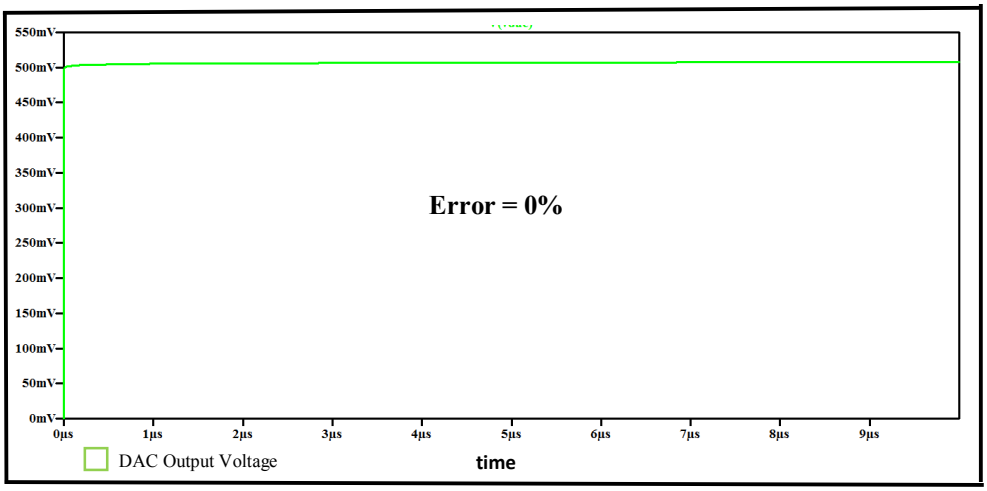


Figure 4.5 DAC output voltage for (1000 0000) digital input

Chapter 5

Successive Approximation Register

5.1 Introduction

A wide range of applications in many different areas such as biomedical applications and wireless communication systems require low power and medium resolution ADC. As mentioned in chapter one, the SA-ADC has received a great interest among many other ADC architectures because of its efficiency in this kind of applications. This kind of ADC is based on the binary search algorithm which will be explained in this chapter. The successive approximation register (SAR) is the digital controller circuit which is responsible for executing the binary search algorithm technique.

The SAR controller is the last block of the ADC components in which the output of the SA-ADC circuit will be determined according to the comparator output. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system.

The main sources of power consumption in this converter come from the comparator, DAC, and the SAR logic [5]. In this chapter, the power consumption in the SAR logic will be discussed and show how the clock system is one of the most power consuming components. The objective of this chapter is to introduce the conventional SAR and the clock gated SAR. Both SARs were studied, simulated and compared. The simulation was on LT Spice IV using 90nm CMOS technology in low voltage operation (supply voltage is 1V). Furthermore, they tested in medium (100 KHz) clock frequency and it was evaluated using D-flip flop (D-FF) and hybrid latch-flip flop (HL-FF). This chapter is organized as follows: Section 5.2 illustrates the conventional SAR circuit. A clock gated SAR circuit is presented in section 5.3. Simulation results are illustrated in section 5.4.

5.2 Conventional SAR

In general, the SAR controller design consists of two registers: one register is for storing the conversion results and another one for estimating the results. The conventional SAR controller is a non-redundant design where for n-bit ADC, n-flip flops are needed which achieves minimum number of flip flops (FF) and minimizes the area of the controller [2].

Figure (5.1) illustrates the conventional SAR controller block diagram. Each control unit and the multiplexer circuit are illustrated in Figure (5.2) and Figure (5.3) respectively. Figure (5.4) shows D-flip flop (D-FF) [2] or hybrid-latch flip flop (HL-FF) [28] which shown in Figure (5.5) can be used or any other FF type can be used. Table (5.1) shows the SAR controller algorithm which illustrates the relation between the data inputs and the FF operation. The initial step of the operation starts by setting the MSB to 1 and other bits to 0. Based on the comparator output, the SAR controller will set the MSB. If the output of the comparator is high, the MSB is set to 1, otherwise, the MSB value is set to 0. This procedure is repeated for all bits until the output word is determined. Hence, starting from the second cycle in the SAR operation, a generic FF (kth) is connected to a multiplexer to be able to select between three data inputs coming from [2,5]:

- The output of the (k+1)th FF (shift right).
- The output of the comparator (Cmp) (data load).
- The output of the (kth) FF itself (memorization).

The output of each control unit in each cycle is given by the following equation [2]:

$$\mathrm{Bit(j)_{next}} = \overline{\mathrm{Mem}}\ \mathrm{X}\ \overline{\mathrm{Bit(j)}}\ \mathrm{X\ Shift} + \mathrm{Bit(j)\ X\ Load} + \mathrm{Mem\ X\ Bit(j)} \qquad (5.1)$$

Where (load) is the comparator's output, (shift) is the value of the previous bit. A chain of OR gates is added up to stop the conversion (Mem) and the conversion results can be stored in the SAR (Bit(j)) [2,5].

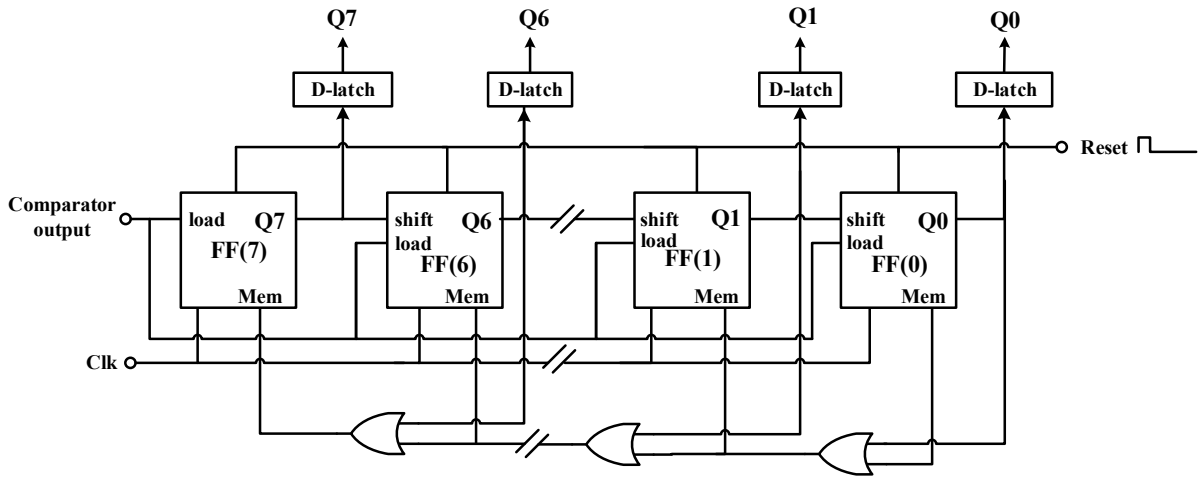


Figure 5.1 Conventional SAR logic block diagram [2]

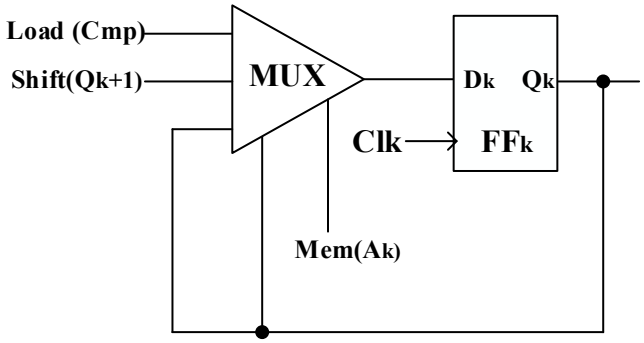


Figure 5.2 Control unit (FF) [5]

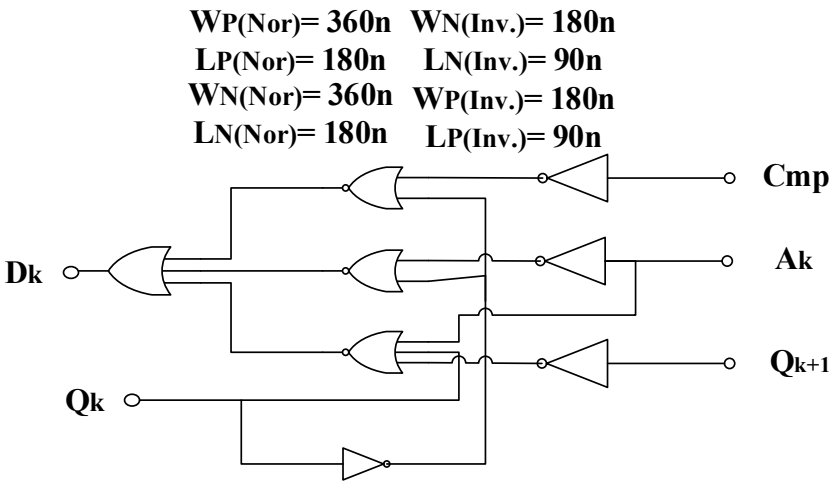


Figure 5.3 Multiplexer circuit [2]

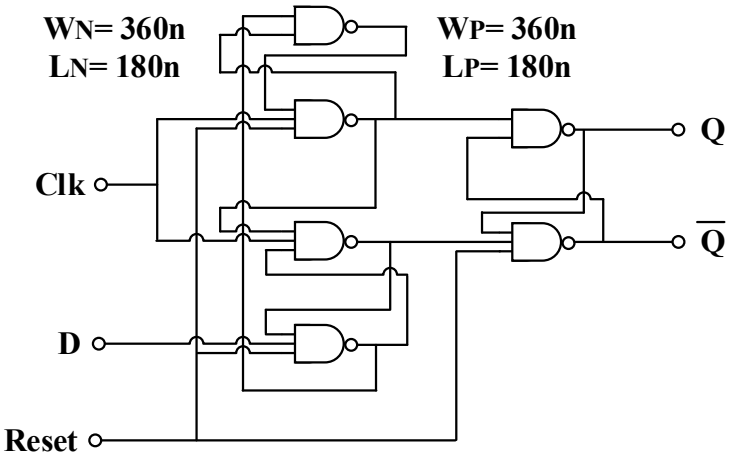


Figure 5.4 D-FF unit [2]

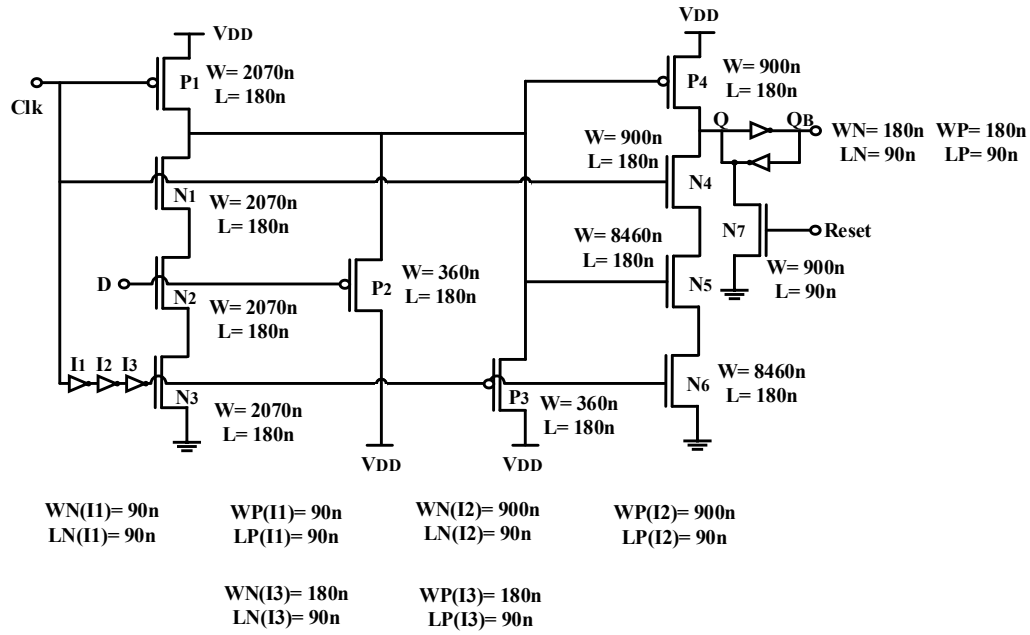


Figure 5.5 HL-FF unit [28]

Table 5.1 SAR controller algorithms [5]

Cycle	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	Comparator output
0	1	0	0	0	0	0	0	0	a_7
1	a_7	1	0	0	0	0	0	0	a_6
2	a_7	a_6	1	0	0	0	0	0	a_5
3	a_7	a_6	a_5	1	0	0	0	0	a_4
4	a_7	a_6	a_5	a_4	1	0	0	0	a_3
5	a_7	a_6	a_5	a_4	a_3	1	0	0	a_2
6	a_7	a_6	a_5	a_4	a_3	a_2	1	0	a_1
7	a_7	a_6	a_5	a_4	a_3	a_2	a_1	1	a_0
Output	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	-

It can be noticed from the conventional SAR operation shown in Figure (5.1) and Table (5.1) that each FF needs **n** clock cycles to finish the conversion. It means that, the whole register needs $\mathbf{n^2}$ clock pulses. Many of these pulses are consuming power without any effect on the FF state, noting that each FF changes its state once or twice during the entire conversion process. Section 5.3 introduces a clock gated based SAR which can solve the conventional SAR problem and minimize the power consumption [5].

5.3 Clock Gated SAR

Figure (5.6) shows a modified block diagram of a clock gated SAR control logic which reported in [5]. The main concept is to insert a logic block and to connect its output to the FF clock terminal Clkg and to connect the FF inverted output terminal to its input terminal (D). As a result, the gated clock signal Clkg will be active only if the FF needs to change its state. Otherwise, the gated clock signal will never be activated, and the FF will hold its state. In this case, the original clock signal Clk will be isolated and it flips its state according to its frequency and does not consider the activity of the FF input signal. Therefore, a non-redundant clock cycles and lower power consumption will be occurred [5].

The required clock propagation for each FF is done by the logic blocks which are the controllers. As shown in Figure (5.6), the modified clock gated SAR logic consists of n-FFs and (n+1)/3 controllers. Each controller is assigned for a specific set of FFs in order to generate gated clock signals. The inverted output of each FF is connected to the corresponding controller and to the input terminal of the FF to implement the toggling operation. Each FF is triggered at the positive edge of its gated clock signal Clkg. Controller 1 and controller 2 are shown in Figure (5.7) and Figure (5.8) respectively. Each controller has gating overhead circuits which are shown in Figure (5.9) and Figure (5.10). They consists of passing transistors which responsible for clock propagation for each FF. The MSB changes its state only when it loads its zero value data { ***Q(n-1) = 1, Cmp = 0 : (data load)*** }. Furthermore, each other bit changes its state when it loads its true data (zero value) or when it receives the data coming from the adjacent FF (shift right) { ***Q(k) =0, Q(k+1)=1 : (shift right) and Q(k) = 1, Cmp = 0 : (data load)*** }. A simple AND logic is added in order to initialize the MSB to 1 as shown in Figure (5.6) [5].

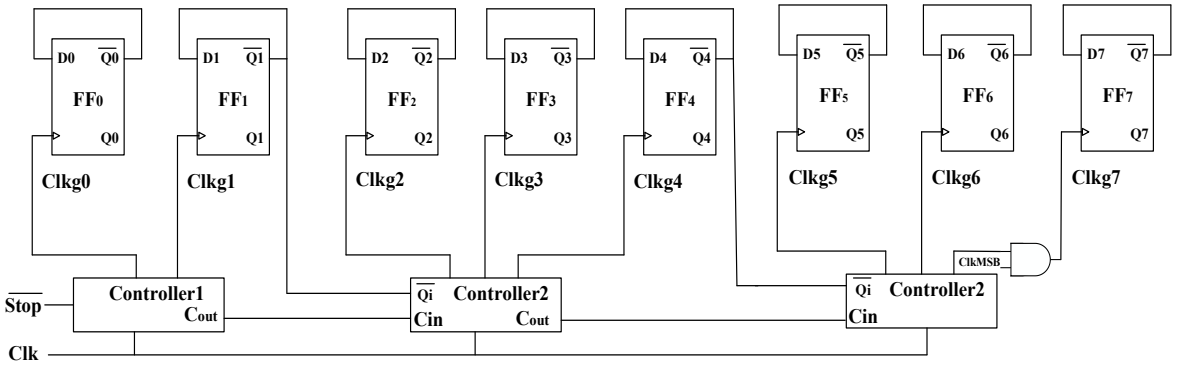


Figure 5.6 Modified clock gated SAR logic block diagram [5]

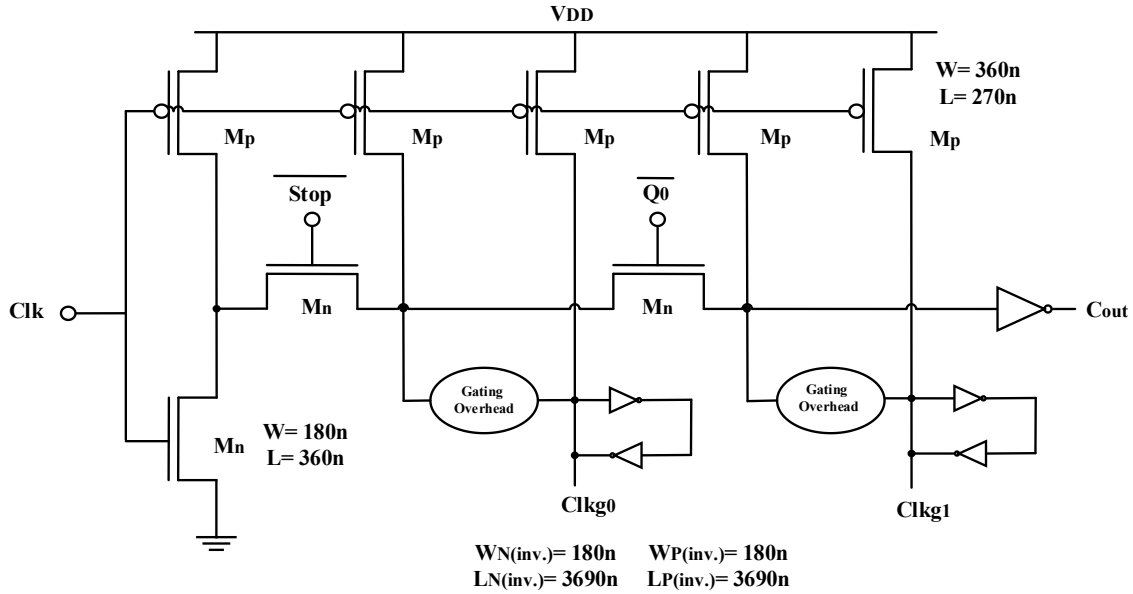


Figure 5.7 Schematic diagram of controller1 [5]

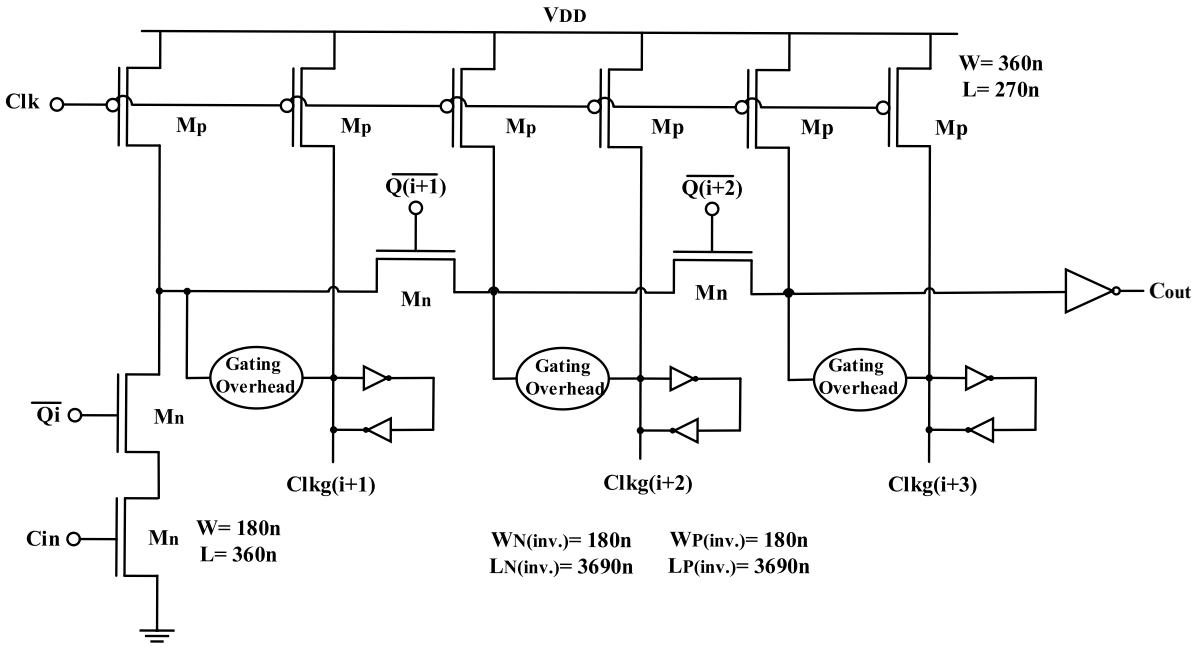


Figure 5.8 Schematic diagram of controller2 [5]

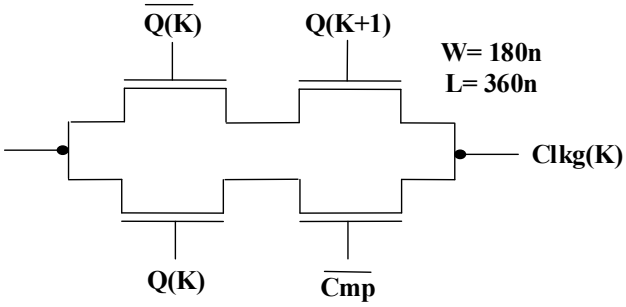


Figure 5.9 Gating overhead circuit for Clkg(k) [5]

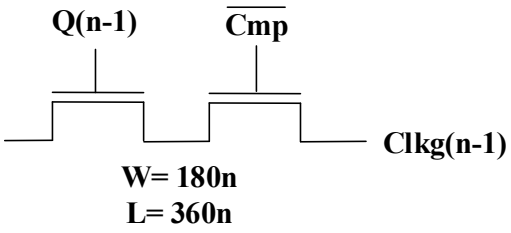


Figure 5.10 Gating overhead circuit for Clkg(n-1) [5]

5.4 Simulation Results

A simulation was done for the conventional and the modified clock gated SAR logic. Figure (5.11) and Figure (5.12) shows the output bits of the conventional SAR logic when the comparator output (Load) is low and high respectively. These outputs are consistent with the theoretically expected outputs and were obtained from the simulation results of the SAR controller. For the modified clock gated SAR logic, Figure (5.13) and Figure (5.14) shows the output bits of the clock gated SAR logic when the comparator output is low (worst case) and high (best case) respectively. All the transistors' aspect ratios for each circuit in both conventional and clock gated SAR controllers are shown in their Figures.

Many different scenarios for the clock gated SAR can be obtained according to the value of the comparator (Cmp) signal. The best scenario is obtained when Cmp signal remains high for the entire conversion process. In this case, Clkg(n-1) remains high and Q(n-1) holds its state. The remaining other gated clock signal will have only one pulse to allow right shifting action as shown in Figure (5.14). Therefore, the total number of clock pulses is decreased to **(n-1)** [5] while in the modified clock gated is **(n)**. The worst scenario is obtained when Cmp signal remains low. In this case, Clkg(n-1) will have only one pulse to allow loading the true data and changing its state from 1 to 0. The remaining other gated clock signal will have two pulses, one to allow right shifting and the other to allow loading the true data as shown in Figure (5.13). Therefore, the total number of clock pulses in this case is reduced to **(2n-1)** [5] while in the modified clock gated is **(2n)**. The difference between the clock gated SAR in [5] and the modified clock gated SAR is one pulse which represents the simple AND logic which responsible for initializing the MSB to 1.

Note that the conventional SAR always needs $\mathbf{n^2}$ pulses for its clock signal. The dynamic power can be calculated as:

$$P = C_L V_{DD}^2 f \alpha \qquad (5.2)$$

Where α represents the switching activity of the signal. It is clear that the switching activity is proportional to $\mathbf{n^2}$ in the conventional SAR while it is proportional to $\mathbf{n}$ in the clock gated SAR. This linear relationship saves a great amount of power especially for a higher resolution register.

In addition to that, the conventional and the clock gated SAR controllers are simulated twice, the first one using D-FF and the second one using the HL-FF for a clock frequency of 100 KHz. The simulation results obtained proves that the clock gated SAR described in [5] saves up to 30.5%

of power consumption compared with the conventional SAR for 100 KHz clock frequency using HLFF. On the other hand it saves 87% for 100 KHz clock frequency using D-FF. Since the objective of this work is to propose a low power SA-ADC for portable biomedical applications. The clock gated SAR has been chosen.

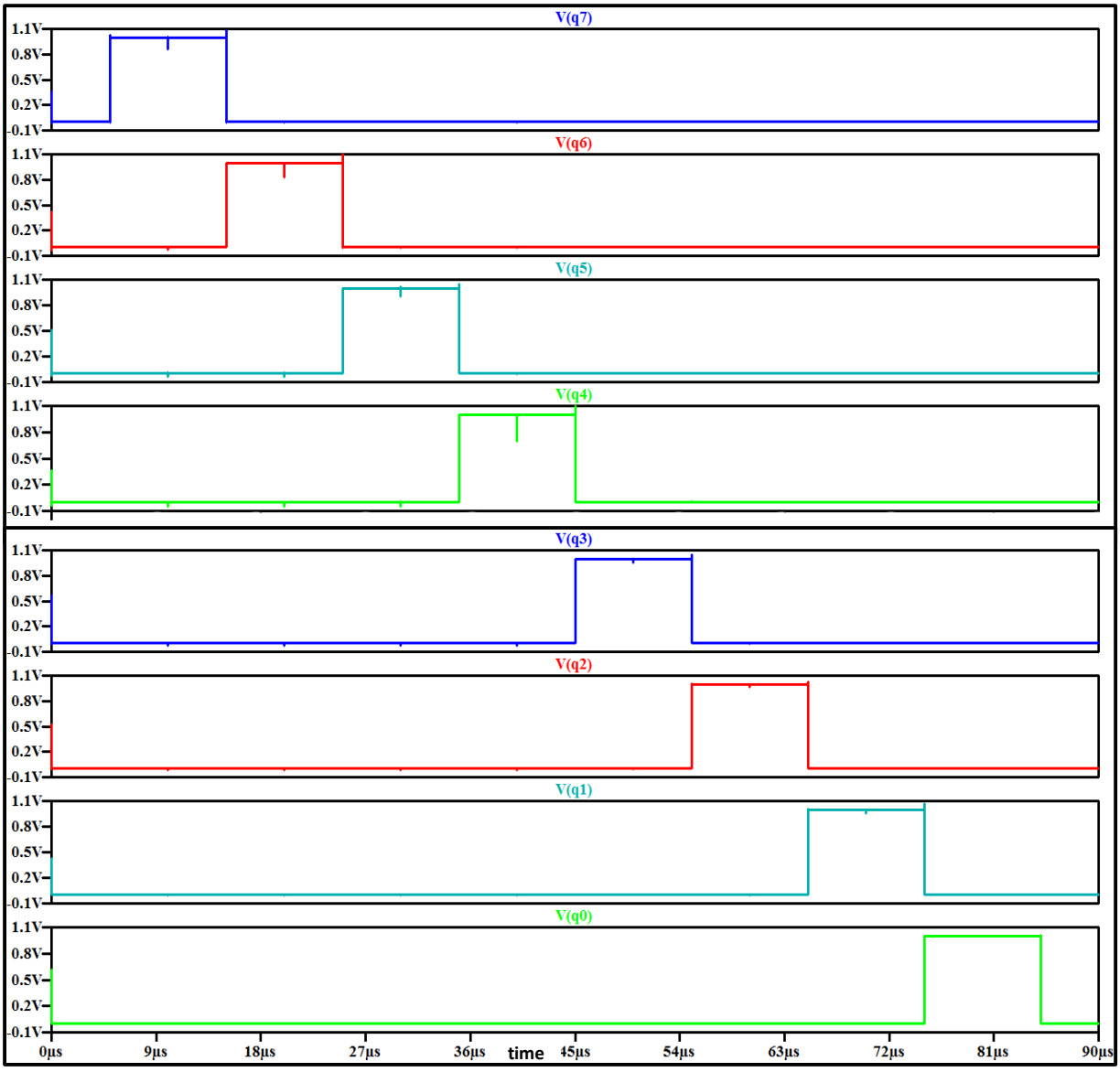


Figure 5.11 Conventional SAR logic outputs when comparator output is 0

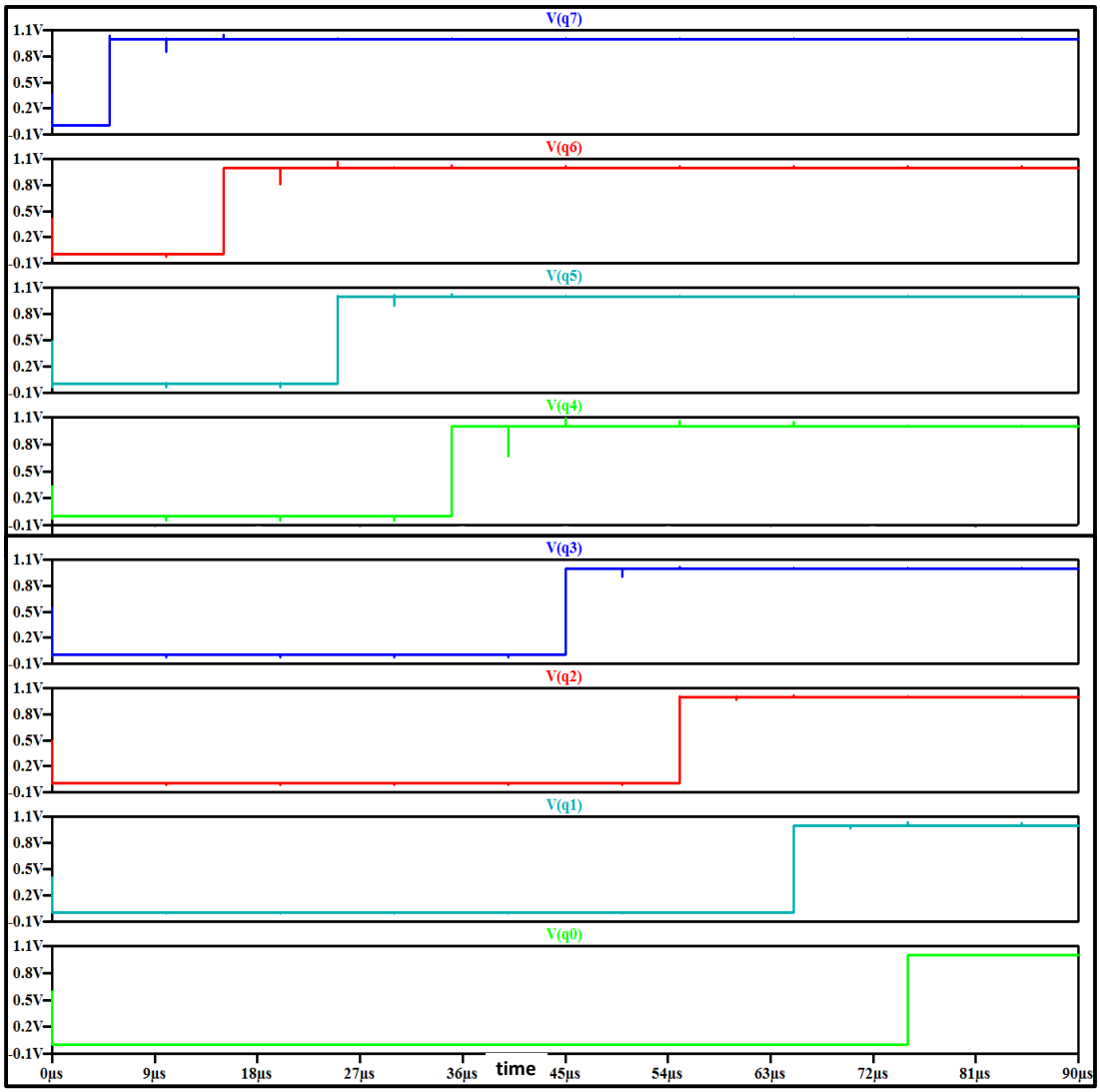


Figure 5.12 Conventional SAR logic outputs when comparator output is 1

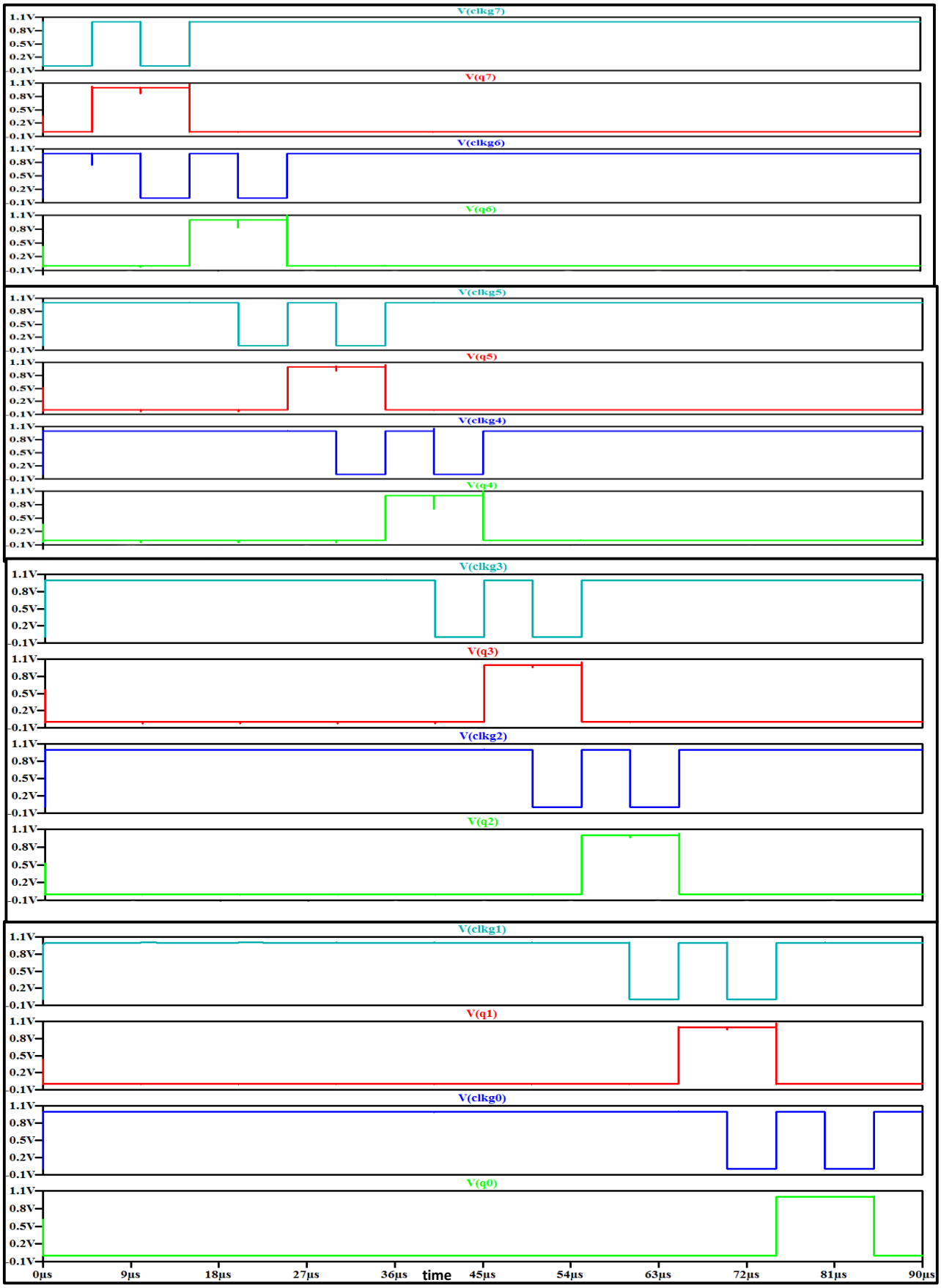


Figure 5.13 Clock gated SAR logic outputs when comparator output is 0 (worst case)

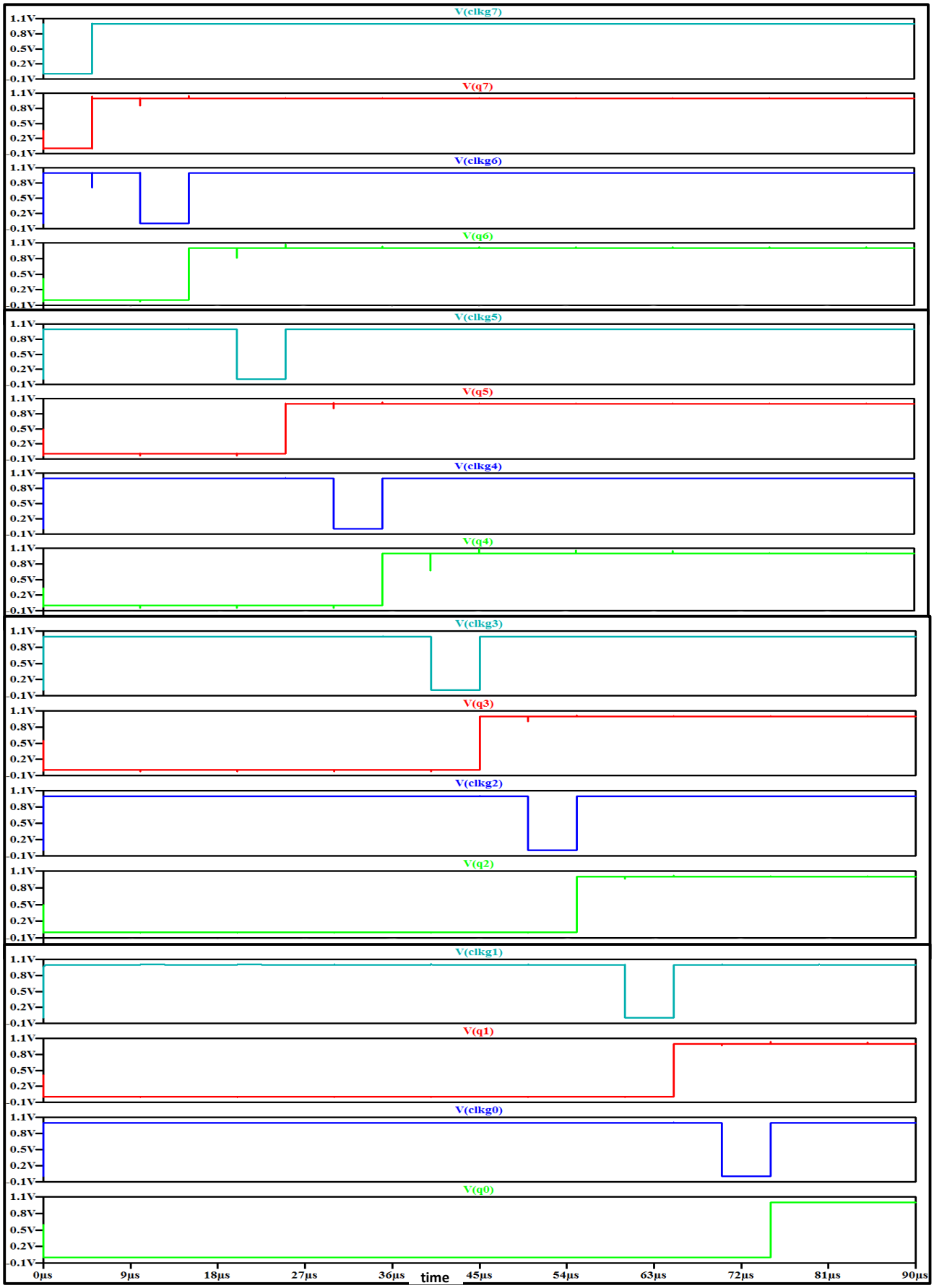


Figure 5.14 Clock gated SAR logic outputs when comparator output is 1 (best case)

Chapter 6

SA-ADC Realizations

6.1 Introduction

Successive Approximation analog-to-digital converter (SA-ADC) has received a great interest in the area of low power and medium resolution ADC because of its high efficiency in this kind of applications. The DAC based SAR ADC and charge redistribution SAR ADC are considered the main two architectures of SA-ADC. As a result from the surveys that have been conducted in the previous chapters on the SA-ADC building blocks; the choice of the SA-ADC building blocks depends on the required application where the desired resolution and sampling rate are balanced with the strengths and weakness such as power consumption, size, cost, and speed.

In this chapter, three different CMOS realizations of an 8-bit SA-ADC will be presented, simulated and compared. These realizations are characterized by moderate speed, moderate accuracy, and low power dissipation which meets the requirements of biomedical applications. Moreover, they are implemented using alternative building blocks that have been discussed in the previous chapters in order to illustrate the effect of each building block structure on the SA-ADC performance especially on the power consumption. In addition to that, the SAR controller for each realization is implemented twice, the first one using D-FF and the second one using the HL-FF. Single ended DAC based SAR ADC architecture has been used.

According to the surveys that have been conducted in the previous chapters; the suitable building blocks have been selected for the first realization which called conventional SA-ADC. These blocks are basic S/H circuit with dummy switch, static comparator, binary-weighted capacitor based DAC, and the conventional SAR logic. In order to achieve further reduction in the power consumption, two more realizations have been proposed. These three SA-ADC realizations are designed using HL-FF unit or D-FF unit. The proposed SA-ADC realizations were simulated using 90nm CMOS technology on LT Spice IV for a 250 Hz-500 mV_{p-p} sinusoidal input with sampling frequency of 10 KS/s and speed of 100 KHz. The supply voltage is 1V.

This chapter is organized as follows: Section 6.2 illustrates the Complete CMOS realizations of an 8-bit SA-ADC and the simulation results are shown in section 6.3.

6.2 8-Bit CMOS SA-ADC Realizations

Figure (6.1) illustrates the schematic diagram of the proposed conventional SA-ADC (realization 1). As mentioned above, it consists of basic S/H circuit with dummy switch (see Figure 2.9 in Chapter 2), static comparator (see Figure 3.2 in Chapter 3), binary-weighted capacitor array based DAC (see Figure 4.1 in Chapter 4) and conventional SAR logic (see Figure 5.1 in Chapter 5). This realization has been simulated using D-FF or HLFF (see Figure 5.4 and Figure 5.5 in Chapter 5). Each of these circuits has been introduced briefly in the previous chapters.

The traditional binary-weighted capacitor array based DAC has been selected instead of the other topologies which were mentioned in Chapter 4. Because the simulation results which obtained from the previous chapters show that the power consumption in the comparator and SAR controller is greater than the power consumption in the DAC. As a results, this thesis is focused on choosing a power efficient structure of comparator and SAR controller in order to save a great amount of power. In addition to that, although, the split capacitor array DAC and the serial charge redistribution DAC are reducing the switching energy, however, they are not compatible with the design of the clock gated SAR controller which has a great effect on reducing the dynamic power consumption. Furthermore, it will increase the clock gated SAR controller complexity which results in more power consumption.

Figure (6.2) illustrates the schematic diagram of the proposed clock gated SA-ADC (realization 2). In order to reduce the power consumption for the control SAR logic as mentioned in chapter 5. The conventional SAR logic has been replaced with the clock gated SAR logic (see Figure 5.6 in Chapter 5) in realization 2. The clock gated SA-ADC realization was simulated using D-FF or HLFF (see Figure 5.4 and Figure 5.5 in Chapter 5).

Figure (6.3) illustrates the schematic diagram of the proposed low-power clock gated SA-ADC (realization 3). In realization 3, the static comparator in realization 2 has been replaced with the double-tail dynamic latched comparator (see Figure 3.10 in Chapter 3) in order to achieve further reduction in the power consumption as mentioned in chapter 3. Furthermore, realization 3 was simulated using D-FF or HLFF (see Figure 5.4 and Figure 5.5 in Chapter 5).

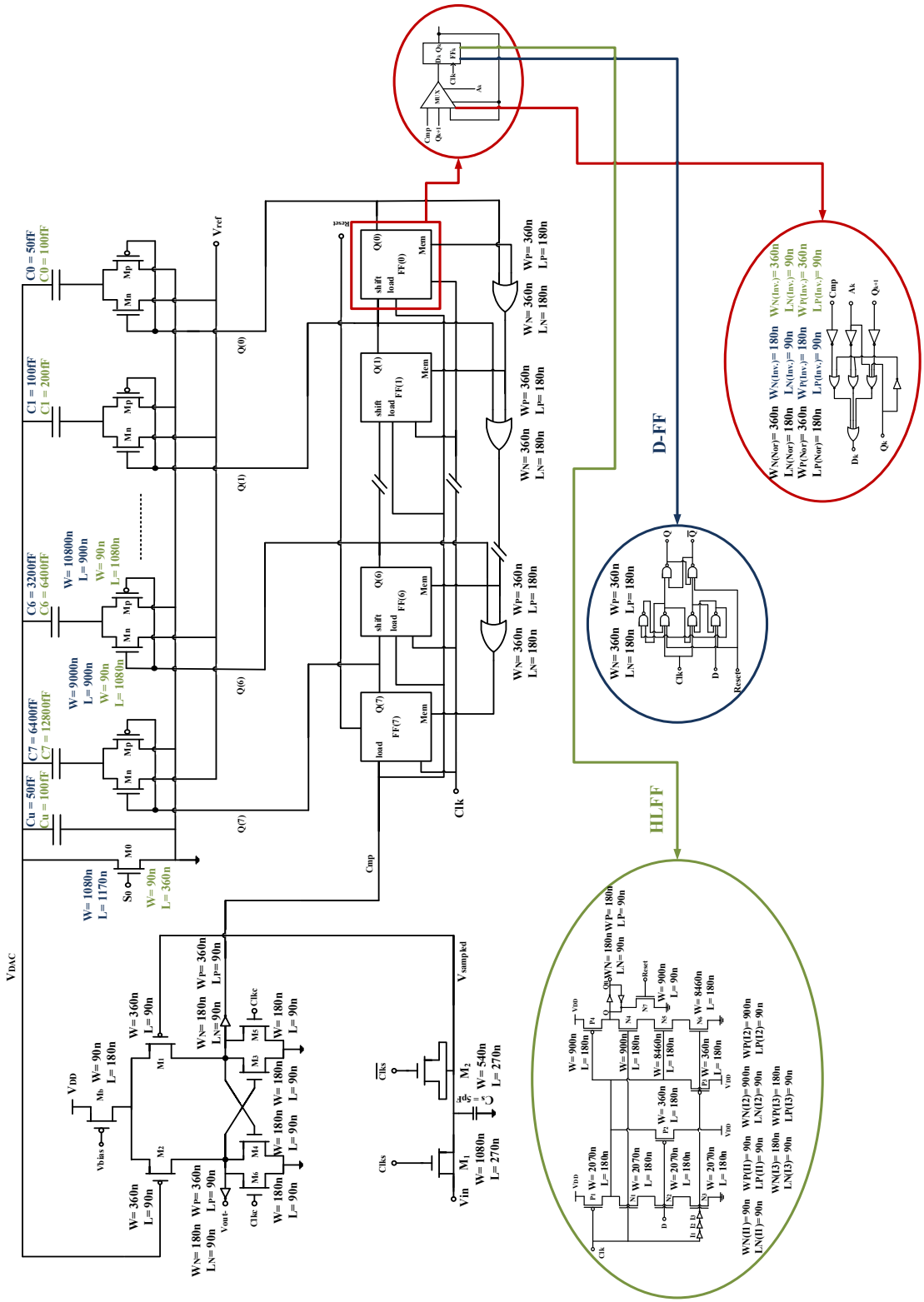


Figure 6.1 Conventional SA-ADC (realization 1)

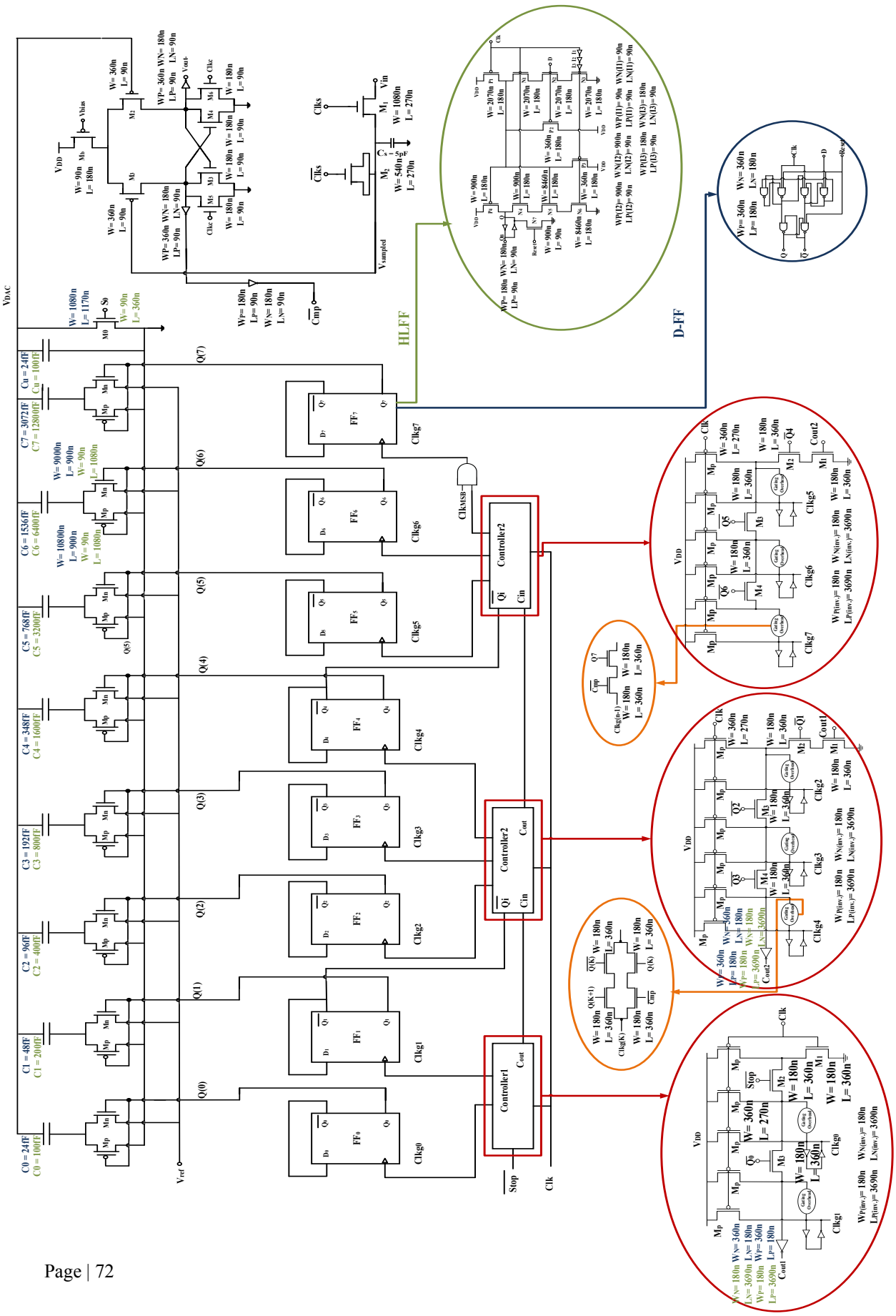


Figure 6.2 Clock gated SA-ADC (realization 2)

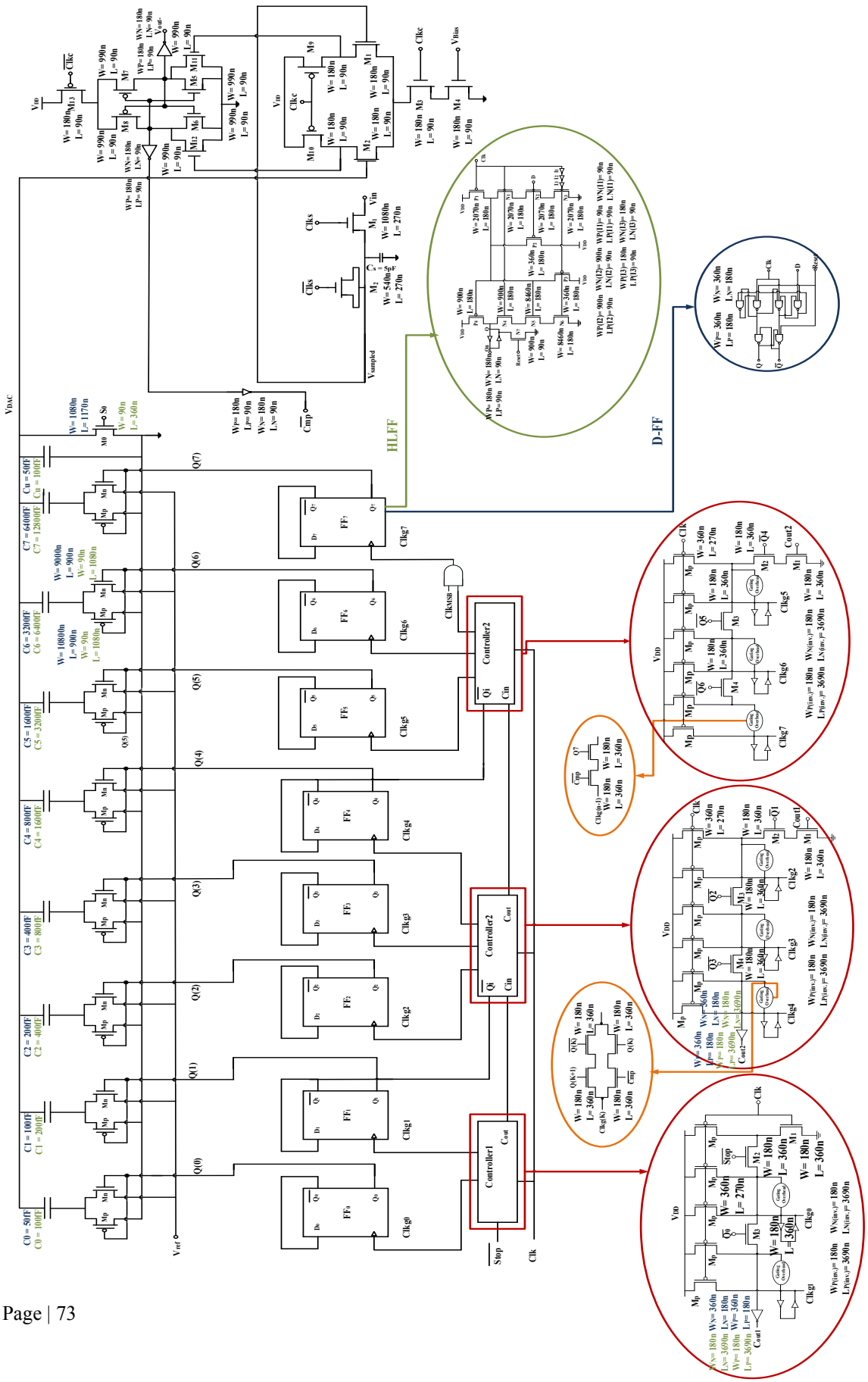


Figure 6.3 Low-power clock gated SA-ADC (realization 3)

6.3 Simulation Results

These three SA-ADC realizations are simulated using D-FF or HL-FF unit. The proposed SA-ADC realizations were simulated using 90nm CMOS technology on LT Spice IV for a 250 Hz-500 mV_{p-p} sinusoidal input which meets the requirements of biomedical (low-frequency) applications [2]. The sampling frequency is 10 KS/s and the speed is 100 KHz under supply voltage of 1V.

In order to evaluate the performance of the proposed SA-ADC realizations, the input signal should be reconstructed from its digital output. The reconstruction method done by feeding the digital output to DAC and low pass filter respectively. Different dynamic performance metrics were measured and calculated for the proposed realizations such as signal-to-noise ratio (SNR) in equation (6.1), spurious-free dynamic range (SFDR) in equation (6.2) and signal-to-noise and distortion ratio (SNDR) in equation (6.3). They were calculated from the fast Fourier transform (FFT) spectrum of the reconstructed signal at the Nyquist input frequency along 100 cycles for full scale input sinusoidal signal. Furthermore, static performance metrics such as the differential non-linearity (DNL) and integral non-linearity (INL) errors were calculated (see Appendix A and Appendix B). The S/H circuit in the three realizations achieves SNDR of 66.65 dB. Figure (6.4) shows the input and the reconstructed sinusoidal signal for realization 1 using D-FF. Realization 2 and 3 have the same shape of the input and the reconstructed sinusoidal signal but the difference between them are the dynamic and static performance metrics which will be illustrated in this section. Figures (6.5), (6.6), and (6.7) show the FFT spectrum of realization 1, 2 and 3 using D-FF or HL-FF respectively.

$$\text{SNR (dB)} = 20\log\frac{\text{Signal}}{\text{Noise}} \tag{6.1}$$

$$\text{SFDR (dB)} = 20\log\frac{\text{Signal}}{\text{Highest Distortion}} \tag{6.2}$$

$$\text{SNDR (dB)} = 20\log\frac{\text{Signal}}{\text{Distortions+Noise}} \tag{6.3}$$

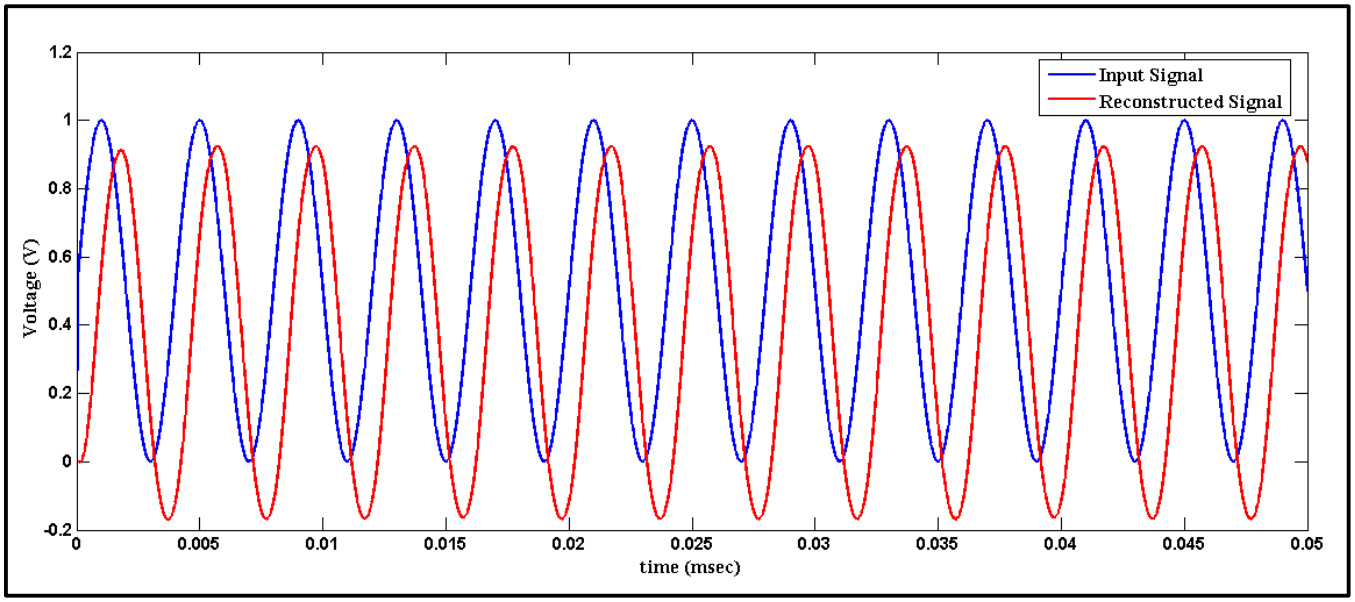


Figure 6.4 The input sinusoidal signal and the reconstructed signal of realization 1 using D-FF

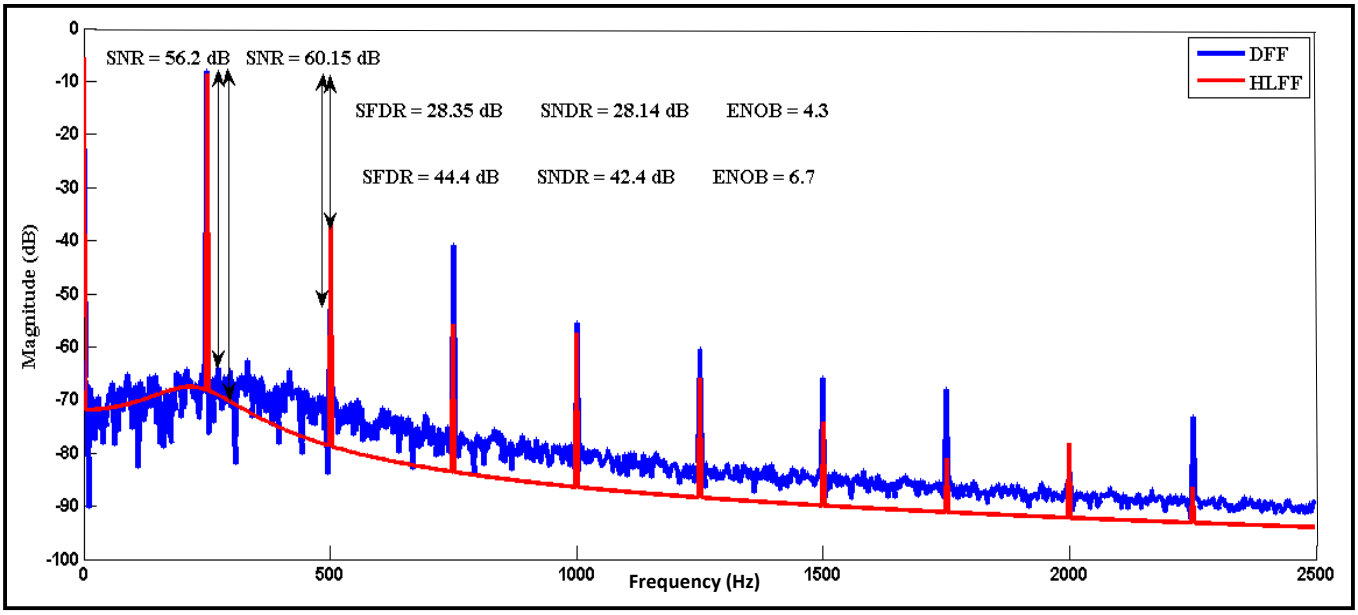


Figure 6.5 FFT spectrum of realization 1 using D-FF or HL-FF

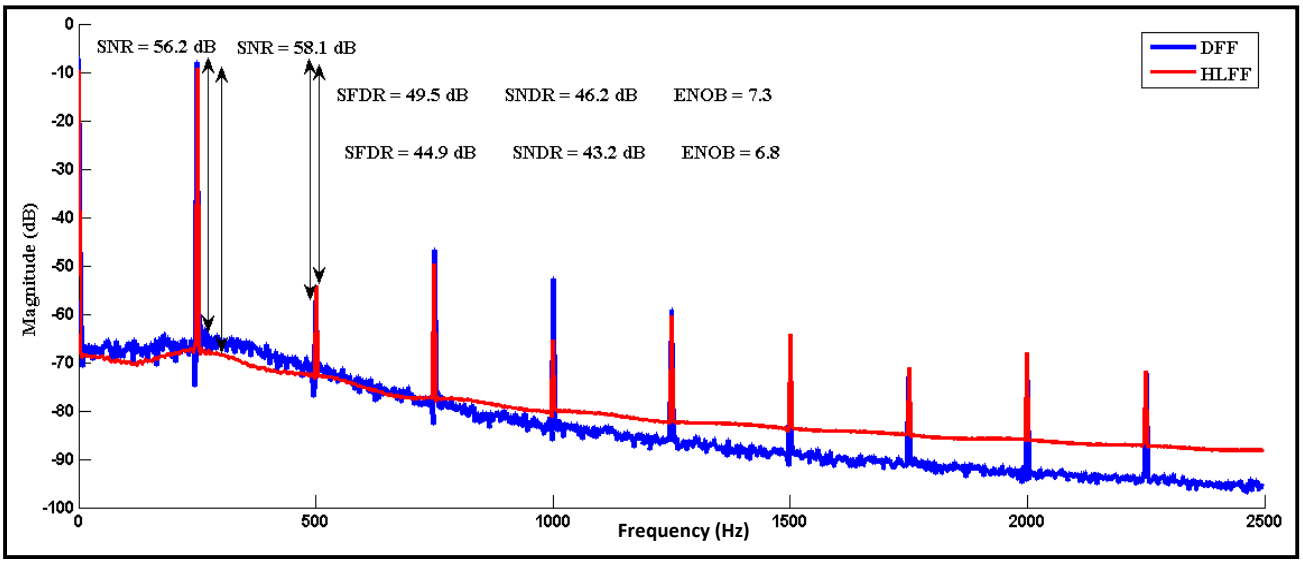


Figure 6.6 FFT spectrum of realization 2 using D-FF or HL-FF

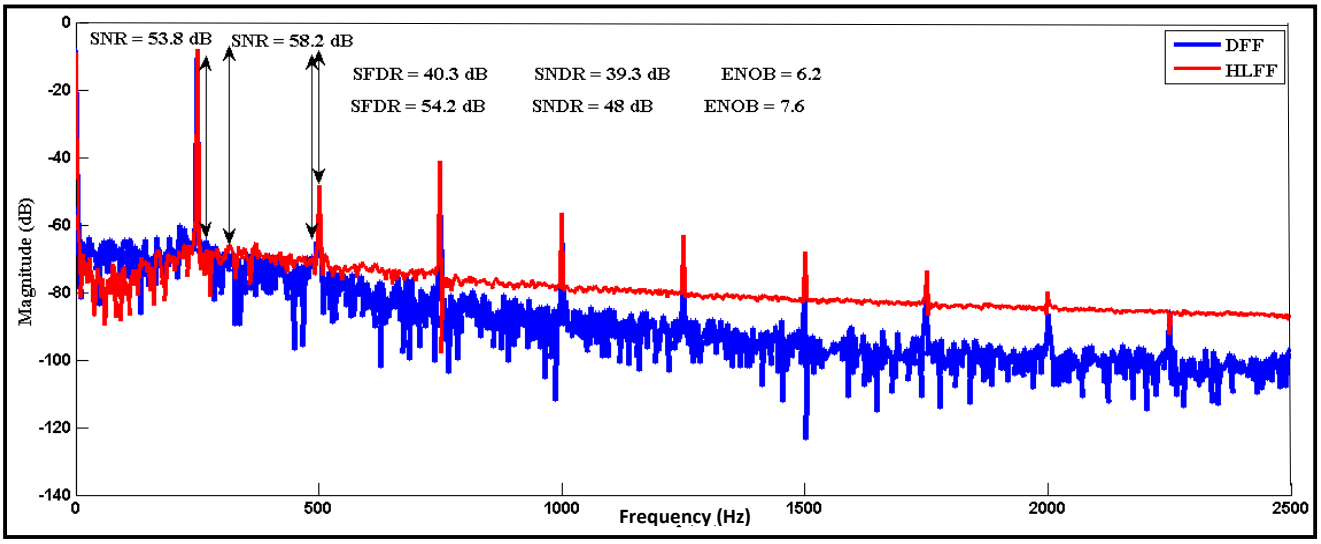


Figure 6.7 FFT spectrum of realization 3 using D-FF or HL-FF

Figures (6.8), (6.9) and (6.10) show the (DNL) and (INL) errors for realization 1, realization 2 and realization 3 respectively using D-FF or HL-FF. The effective number of bit (ENOB) is calculated based on ENOB = ((SNDR−1.76) / 6.02). One more important parameter of the ADC is the figure of merit (FOM_1) and (FOM_2), which is calculated based on the following equations (6.4) and (6.5) [2]:

$$\mathrm{FOM}_1 = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}*2*\mathrm{ERBW}}} \tag{6.4}$$

$$\mathrm{FOM}_2 = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}*\mathrm{fs}}} \tag{6.5}$$

Where ERBW is the effective resolution bandwidth [2]. In addition to that, the power consumption was measured for the proposed realizations. Table (6.1) shows the power consumption percentage for each ADC building block in realization 1, 2 and 3. For example, in realization 1, the S/H circuit does not have supply voltage and the required power to turn the switch ON and OFF has been neglected. The comparator, DAC and SAR controller circuits in realization 1 consume 55%, 8% and 37% of the total ADC power consumption respectively using D-FF. On the other hand, for realization 1, they are consume 25%, 4% and 71% of the total ADC power consumption respectively using HL-FF and similarly for the remaining realizations. Table (6.2) summarizes the simulation results and show the comparison of the proposed 8-bit SA-ADC realizations.

As a result, in any digital circuit, the clock signal is the main source of dynamic power consumption due to its high frequency. Therefore the digital circuit SAR logic considers one of the main sources of power consumption in SA-ADC as discussed in Chapter 5. It can be noticed from the simulation results in Table (6.2) that after the clock gated SAR logic is used in realization 2, the total power consumption of the SA-ADC is reduced by 23.9% and 35.3% using HL-FF and D-FF respectively. The second main source of power consumption is the comparator. In realization 3, a double-tail dynamic latched comparator has been used in order to avoid static power consumption. As a result, it achieves 1.47uW and 200 nW using HL-FF and D-FF respectively with reasonable SNR, SNDR, ENOB and FOM. Therefore realization 3 is the best realization compared with realization 1 and 2 in term of lower power consumption regardless the FF type.

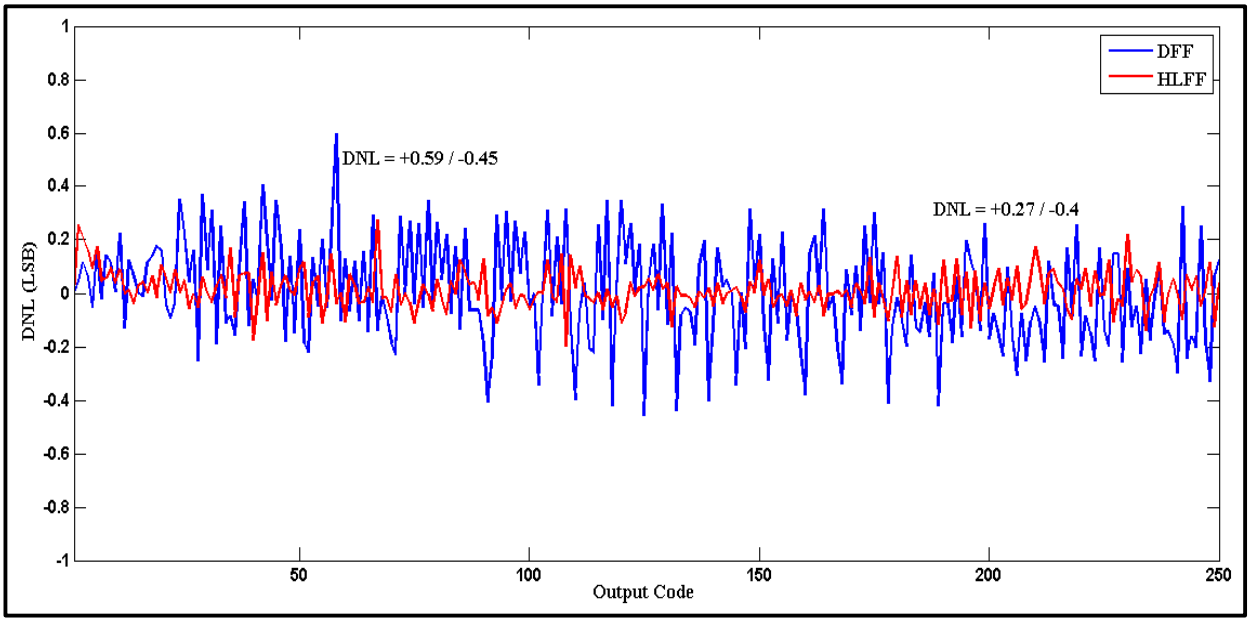
However, HL-FF has been strengthen by increasing transistors aspect ratio in order to maintain the functionality for the SA-ADC. As a result, the second main contribution that obtained in this

thesis, that the FF type which used in the SAR logic has a great effect on the power consumption. The simulation results obtained in Table (6.2) shows that the conventional SA-ADC using D-FF (realization 1 using D-FF) has lower power consumption than the conventional SA-ADC using HL-FF (realization 1 using HL-FF) by 50.5%. Therefore, the best realization among the proposed SA-ADCs is the low-power clock gated SA-ADC using D-FF (realization 3 using D-FF) which achieves 200 nW of power consumption without additional calibration or analog circuits (see Appendix C). From the FFT shown in Figure (6.7), the SNR, SFDR, and SNDR are about 53.8 dB, 54.2 dB and 48dB respectively. It achieves ENOB of 7.6 and FOM_2 of 0.1 pJ/conversion-step. In addition to that, it achieves +0.34/-0.3 LSB of DNL and +0.79/-0.58 LSB of INL as shown in Figure (6.10).

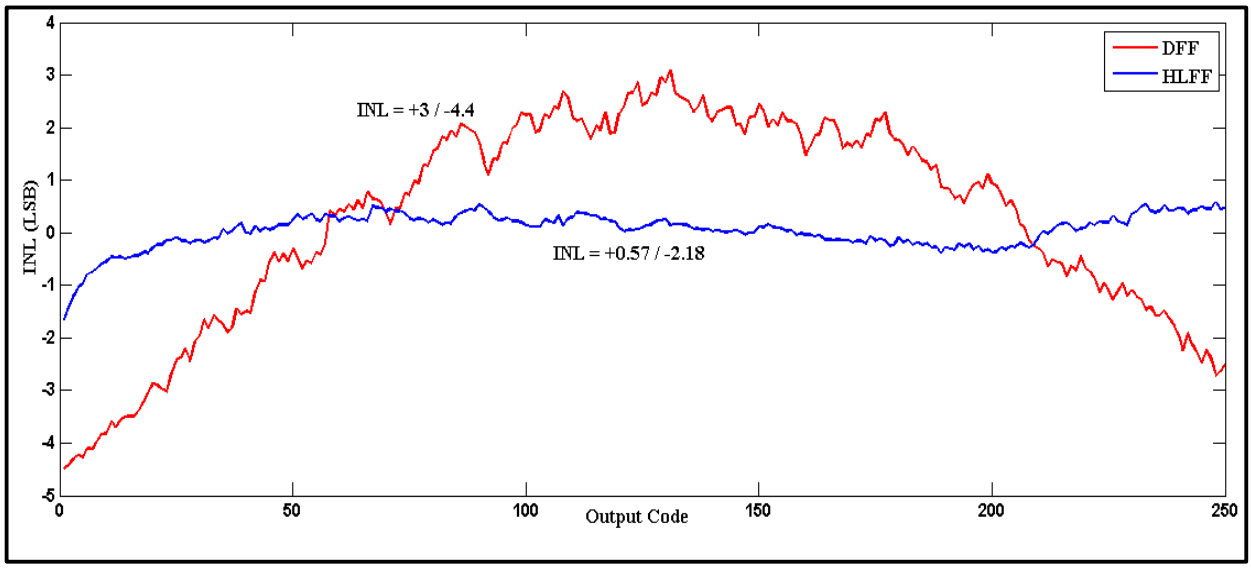
In addition to that, the proposed low-power clock gated SA-ADC using D-FF was tested on 0.85V supply voltage. The latch stage in the double-tail dynamic latched comparator aspect ratios has been changed to W= 540nm and L=90nm. Furthermore, the aspect ratio of the NMOS switch M0 in the binary weighted capacitor array DAC has been changed to W=1080nm and L=2610nm. As a result, it achieves 88.76 nW of power consumption. Figure (6.11) illustrates the FFT spectrum of the low-power clock gated SA-ADC using D-FF under 0.85V supply voltage. It has SNR, SFDR, and SNDR of 54.6 dB, 39.19 dB and 37.92 dB respectively. It achieves ENOB of 6 and FOM_2 of 0.13 pJ/conversion-step. It achieves +0.38/-0.28 LSB of DNL and +0.9/-0.85 LSB of INL as shown in Figure (6.12).

The 8-bit digital codes of the proposed low-power clock gated SA-ADC using D-FF can be used by a digital signal processor to diagnose the brain activities precisely. The proposed 8-bit low-power clock gated SA-ADC using D-FF has been designed, extracted, and simulated in 90nm CMOS technology model file using L-Edit. The layout of the proposed 8-bit low-power clock gated SA-ADC using D-FF realization under 1V supply voltage is shown in Figure (6.13). Furthermore, it was tested on a real recorded beta EEG signal as an example of biomedical signals. Figures (6.14) and (6.15) show the input real recorded beta EEG signal to the SA-ADC and the reconstructed real recorded beta EEG signal from the low-power clock gated SA-ADC using D-FF under 1V supply voltage respectively. Hence, Table (6.3) summarizes the performance of the proposed low-power clock gated SA-ADC using D-FF compared with five other designs reported in the literature. From this comparison, the proposed low-power clock gated SA-ADC using D-FF

design achieves the objective of minimum power consumption with good ENOB and without additional calibration or analog circuits. Furthermore, the clock gated SA-ADC using D-FF unit (realization 2 using D-FF unit) saves up to 55%, 11.5% and 97.4% of power consumption compared with the previous works reported in [2,6,7] respectively. In addition to that, it was accepted in the graduate student research conference in 2016.

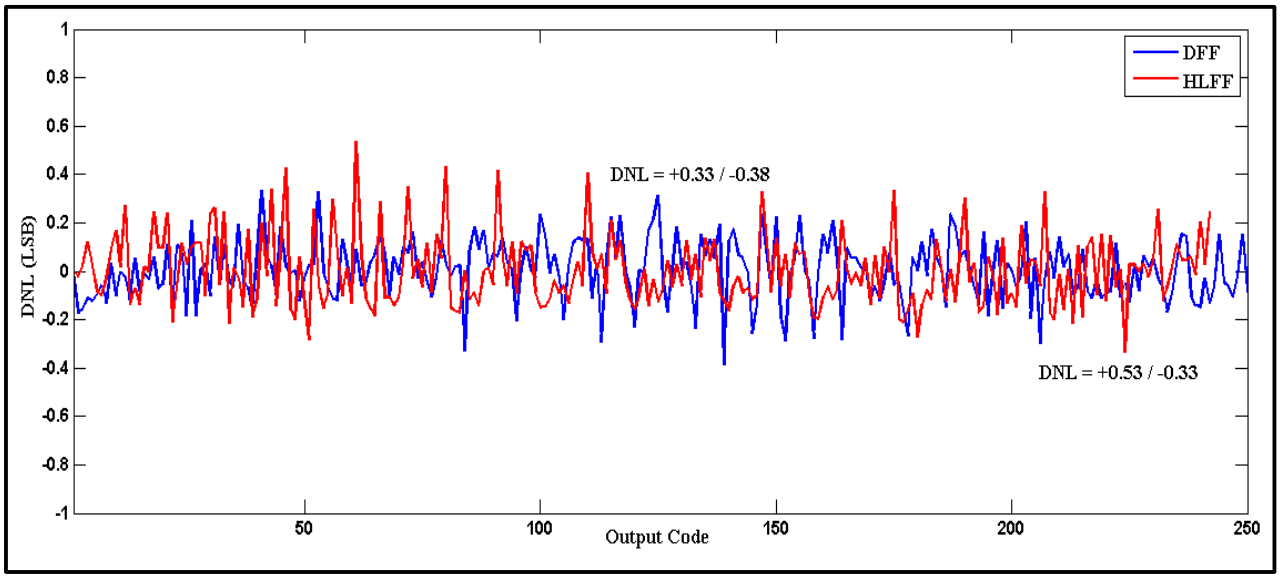


(a)

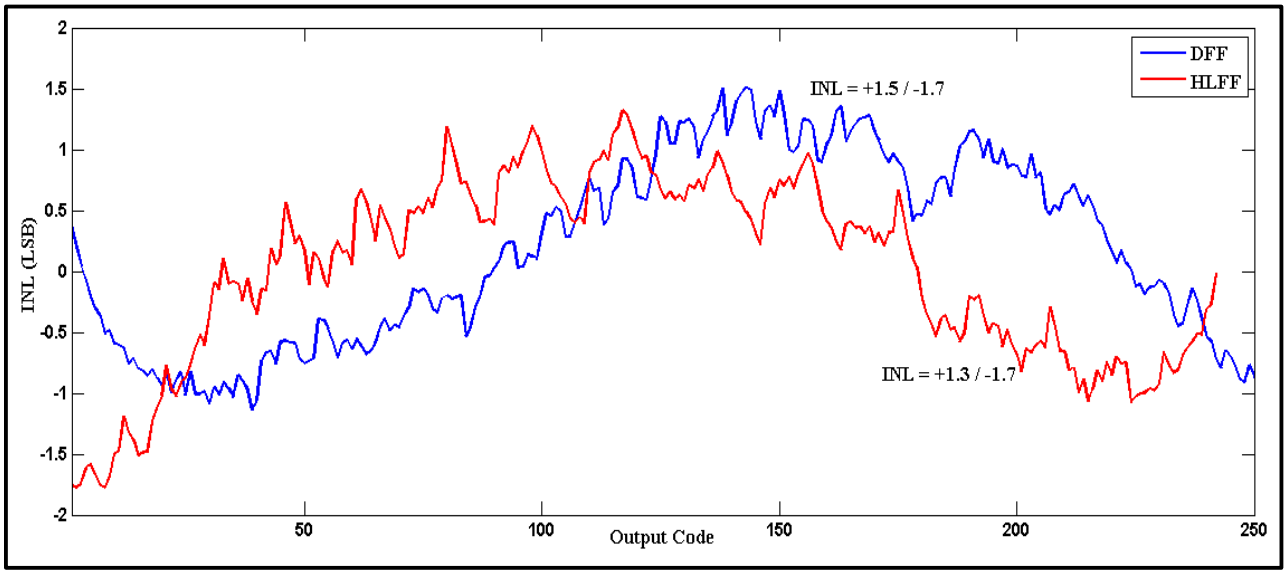


(b)

Figure 6.8 (a) DNL of realization 1 using D-FF or HL-FF (b) INL of realization 1 using D-FF or HL-FF

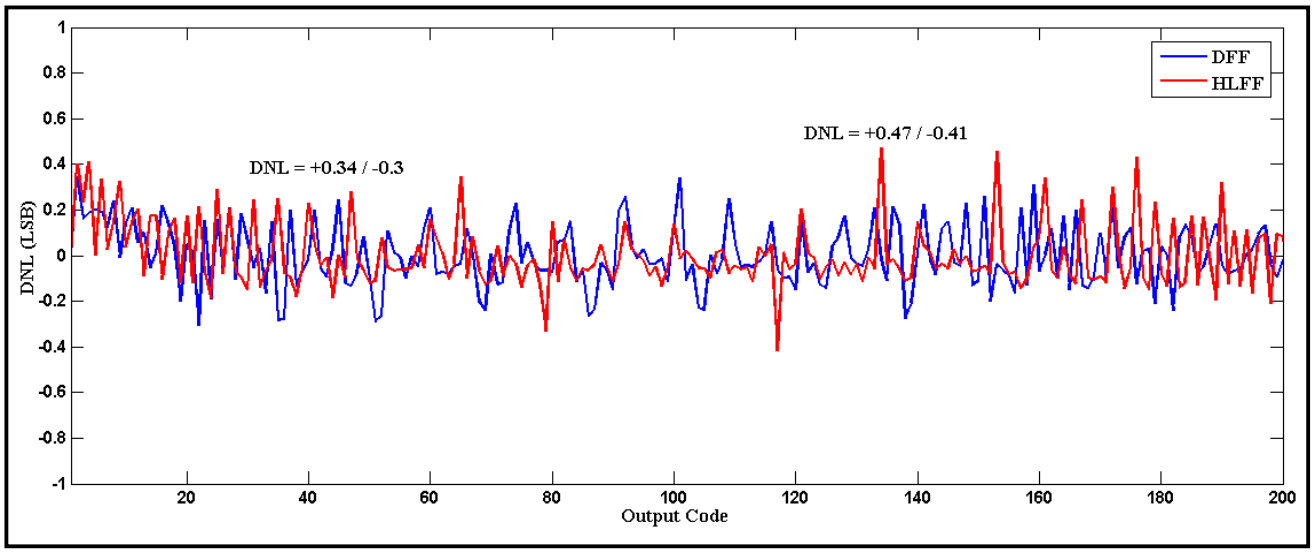


(a)

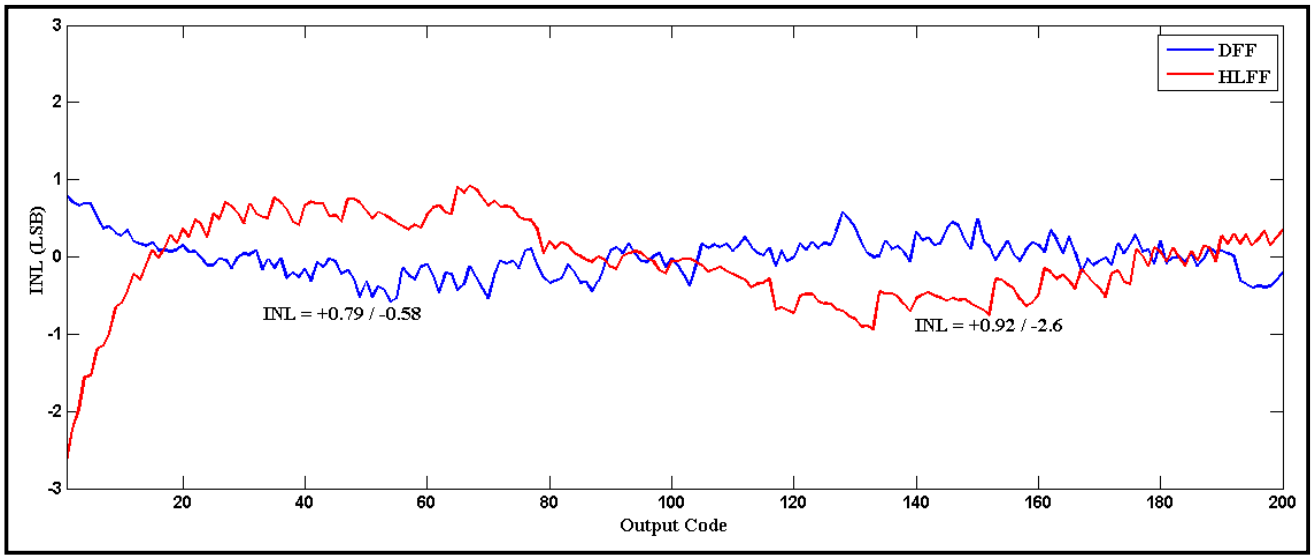


(b)

Figure 6.9 (a) DNL of realization 2 using D-FF or HL-FF (b) INL of realization 2 using D-FF or HL-FF



(a)



(b)

Figure 6.10 (a) DNL of realization 3 using D-FF or HL-FF (b) INL of realization 3 using D-FF or HL-FF

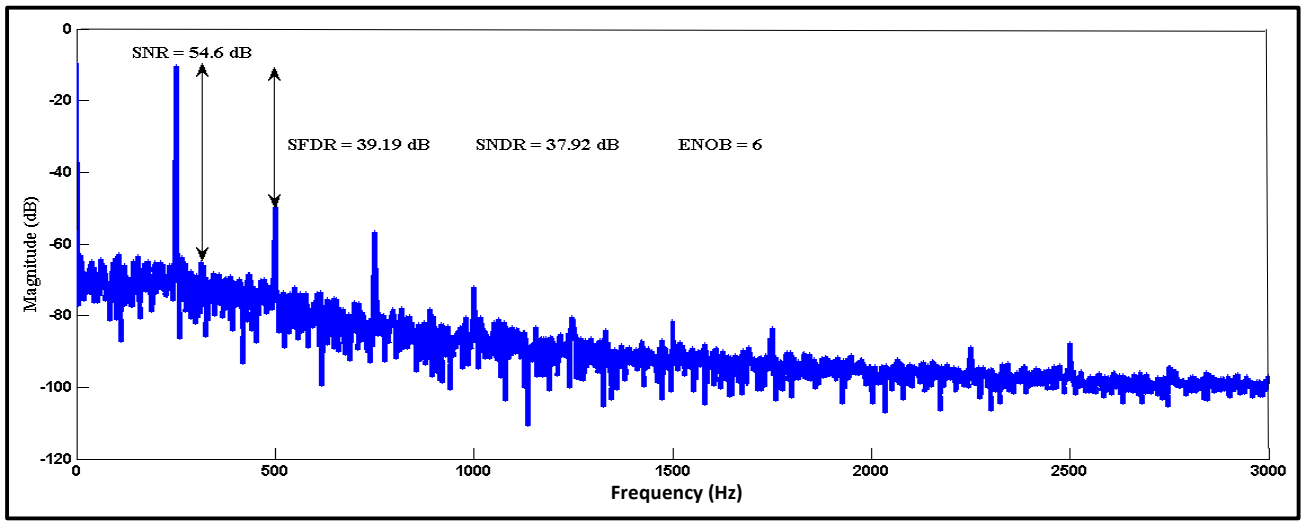
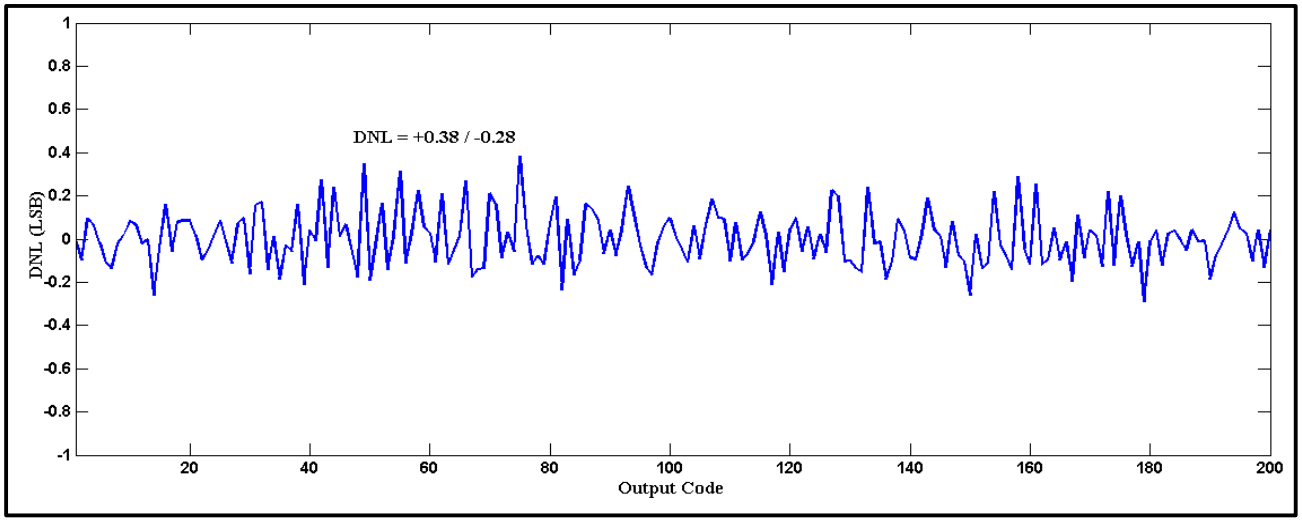
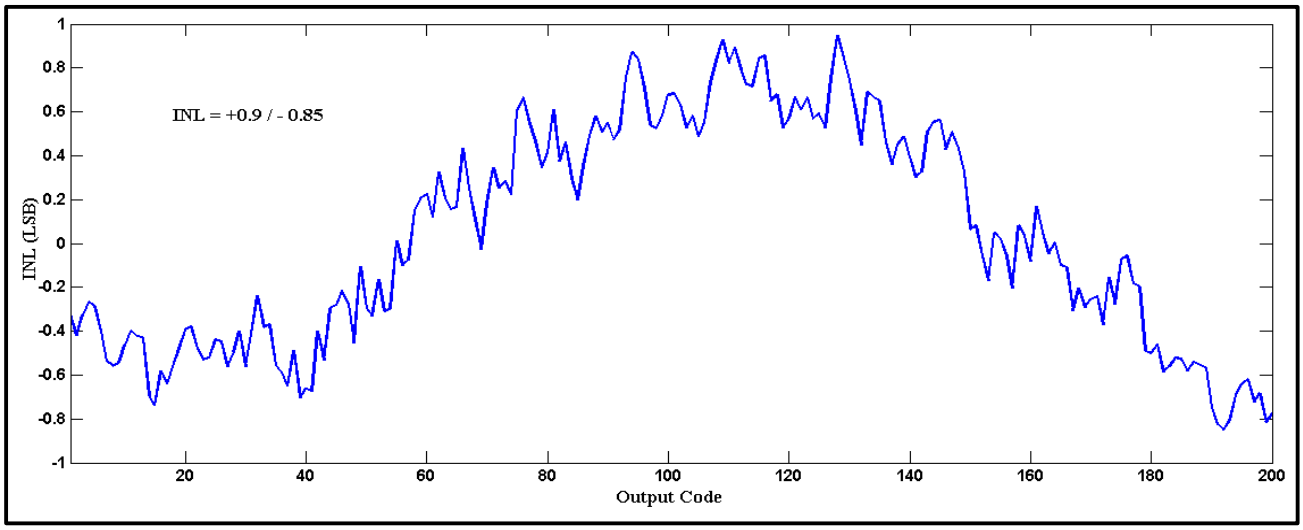


Figure 6.11 FFT spectrum of the proposed low-power clock gated SA-ADC using D-FF under 0.85V supply voltage



(a)



(b)

Figure 6.12 (a) DNL of realization 3 using D-FF under 0.85V supply voltage (b) INL of realization 3 using D-FF under 0.85V supply voltage

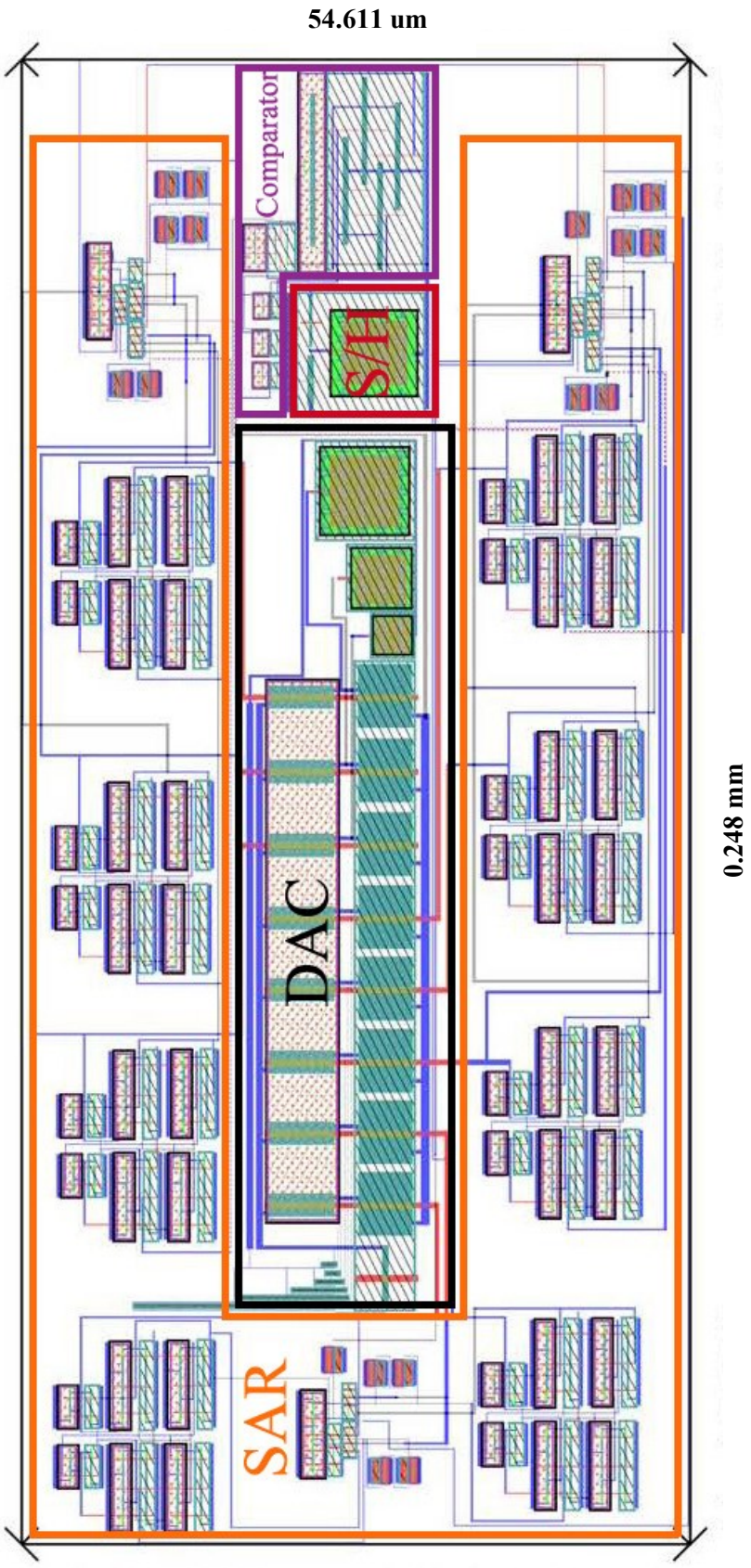


Figure 6.13 The layout of the proposed 8-bit low-power clock gated SA-ADC using D-FF realization under 1V supply voltage

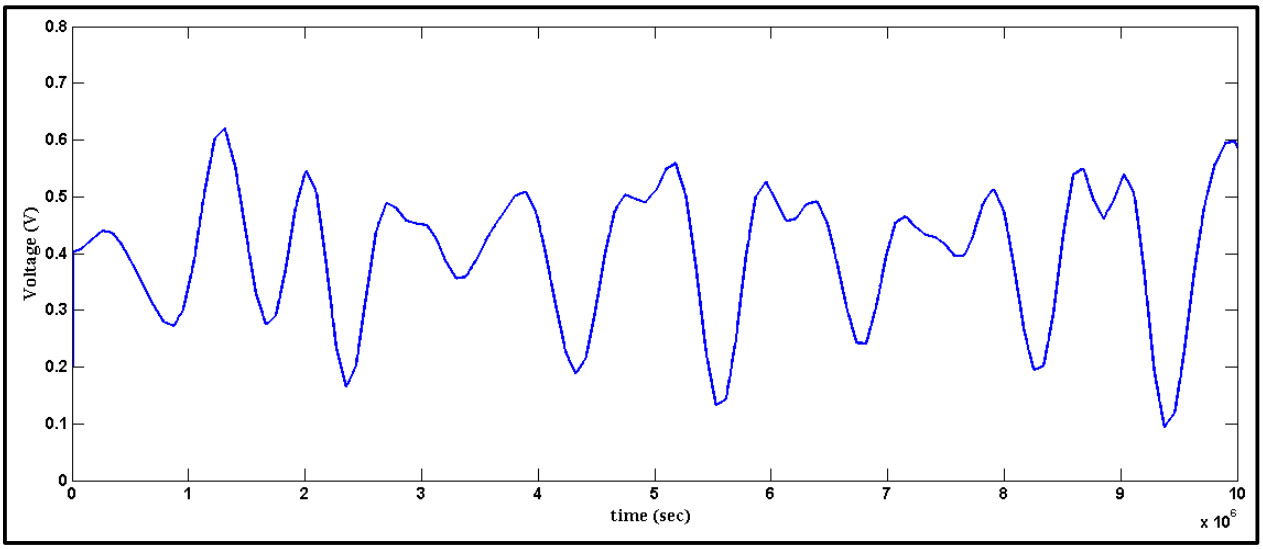


Figure 6.14 Real recorded input beta EEG signal

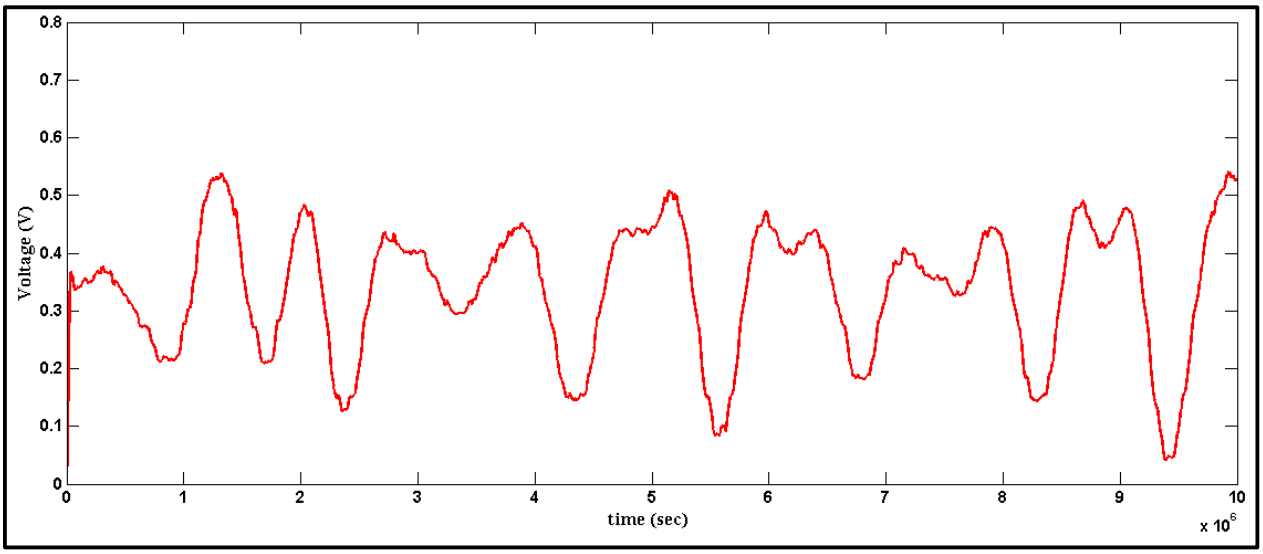


Figure 6.15 Reconstructed real recorded beta EEG signal from low-power clock gated SA-ADC using D-FF realization under 1V supply voltage

Table 6.1 Power consumption percentage for each building block in realization 1, 2 and 3

ADC Realizations	S/H		Comparator		DAC		SAR Logic	
	HL-FF	D-FF	HL-FF	D-FF	HL-FF	D-FF	HL-FF	D-FF
Realization 1	-	-	25 %	55 %	4 %	8 %	71 %	37 %
Realization 2	-	-	35 %	87 %	4 %	9 %	61 %	4 %
Realization 3	-	-	10 %	42.5 %	10 %	42.5 %	80 %	15 %

Table 6.2 Simulation results and comparison of three proposed 8-bit SA-ADC realizations

ADC Realizations / Metrics	90 nm CMOS Technology under 1 V Supply Voltage					
	Realization 1		Realization 2		Realization 3	
	HL-FF	D-FF	HL-FF	D-FF	HL-FF	D-FF
SNR (dB)	60.15	56.2	58.1	56.2	58.2	53.8
SNDR (dB)	28.14	42.4	43.2	46.2	39.3	48
SFDR (dB)	28.35	44.4	44.9	49.5	40.3	54.2
ENOB	4.3	6.7	6.8	7.3	6.2	7.6
ERBW (KHz)	0.65	0.75	0.65	0.75	0.9	0.75
DNL (LSB)	+0.27/-0.4	+0.59/-0.45	+0.53/-0.33	+0.33/-0.38	+0.47/-0.41	+0.34/-0.3
INL (LSB)	+0.57/-2.18	+3/-4.4	+1.3/-1.7	+1.5/-1.7	+0.92/-2.6	+0.79/-0.58
Power Dissipation	2.63 uW	1.3 uW	2 uW	0.84 uW	1.47 uW	200 nW
Total RMS Noise across BW of 500 Hz (nV)	239.85	996.59	944.41	996.59	1010	960.61
FOM_1 (pJ/Conversion-Step)	102.703	8.33	13.8	3.55	11.1	0.68
FOM_2 (pJ/Conversion-Step)	13.35	1.25	1.79	0.53	1.99	0.1

Table 6.3 Comparison with other previous works

Specifications	[2]	[6]	[7]	[8]	[9]	This Work (realization 3 using D-FF)	
Technology	0.25 um	0.18 um	0.18 um	0.13 um	110 nm	90 nm	
Supply Voltage	1 V	1 V	1 V	0.5 V	1 V	0.85 V	1 V
Resolution	8-bit	8-bit	10-bit	11-bit	10-bit	8-bit	8-bit
Sampling Rate (KS/sec)	10	10	40	10 KS/s	20	10	10
SNR (dB)	57	50.5	58.5	-	-	54.6	53.8
SNDR (dB)	40.5	45.2	58.3	61.6	56.5	37.92	48
SFDR (dB)	41	54	-	78	64.7	39.19	54.2
ENOB	6.5	7.2	9.4	9.93	9.1	6	7.6
ERBW (KHz)	1.5	1	0.3	-	-	0.4	0.75
DNL (LSB)	-	-+0.38/-0.41	0.25	+0.96/-0.97	0.44	+0.38/-0.28	+0.34/-0.3
INL (LSB)	-	+0.6/-0.89	0.45	+0.96/-0.98	0.58	+0.9/-0.85	+0.79/-0.58
Power Dissipation	1.87uW	0.95uW	32.6uW	730 nW	100 nW	88.76nW	200 nW
FOM_1 (pJ/Conversion-Step)	6.85	3.23	80.4	-	-	1.73	0.68
FOM_2 (J/Conversion-Step)	2.06 p	0.64 p	1.206 p	74.8 f	9.1 f	0.13 p	0.1 p

Chapter 7

Conclusion

Analog-to-digital converter (ADC) is one of the main electronic blocks in the biomedical systems and healthcare integrated circuit in which it considered one of the main building blocks in data processing applications. Therefore, it has a great effect and it limits the performance of the overall system. Low power design and high resolution ADC are the main requirements in the biomedical applications. Successive approximation analog to digital converter (SA-ADC) is a proper choice for low power ADC.

SA-ADC is one of the most popular approaches for realizing A/D converters, due to their reasonably quick conversion time, moderate circuit complexity, medium accuracy, and it is a proper choice for low power applications. Thus, one of the main challenges in designing SA-ADC is to succeed in proposing low power, simple and accurate design.

The most power efficient SA-ADC is derived from three different possible realizations. These realizations are implemented based on the survey that has been conducted on different structures and design considerations of each building block in the SA-ADC. The different structures of each building blocks has been analyzed, simulated and compared in order to select the best candidate for biomedical (low-frequency) applications in term of low power consumption. As a result, three different CMOS realizations of an 8-bit single ended DAC based SAR ADC are proposed. Moreover, they are implemented using alternative building blocks of the SA-ADC in order to illustrate the effect of each building block structure on the SA-ADC performance especially on the power consumption. The aim of this work is to reduce the power consumption. Therefore, in each realization the power consumption has been minimized using alternative building blocks. Furthermore, in each realization, the SAR controller is implemented twice, the first one using D-flip flop (D-FF) and the second one using the hybrid latch-flip flop (HL-FF).

This chapter is organized as follows: Section 7.1 illustrates the conclusion of each chapter and Section 7.2 presented the future work.

7.1 Conclusion of the Chapters

The results that were obtained from the study which has been conducted in Chapter 2 that in term of high SNDR and low power consumption, the differential basic S/H circuit is the best candidate for low frequency applications, while S/H circuit with bootstrapped technique is the best candidate for medium to high frequency applications. However, the basic S/H circuit with dummy switch was found the best candidate for single ended low power and high SNDR which meets the requirements of biomedical signals.

Chapter 3 concludes that the double-tail dynamic latched comparator achieves the requirements of low power consumption, medium speed and proper dynamic range for biomedical (low-frequency) applications comparing with the other mentioned comparator circuits.

Different DACs topologies have been discussed in Chapter 4. The advantages and disadvantages of each DAC topology has been illustrated. The traditional and simple binary weighted capacitor array DAC has been chosen for the biomedical signals.

Chapter 5, illustrates two different SAR controllers which are the conventional SAR and clock gated SAR. It In this chapter, the conventional SAR and the modified clock gated SAR have been studied, simulated and compared while they were used in the thee different realizations of SA-ADC in Chapter 6 to prove that the modified clock gated SAR saves a great amount of power dissipation with respect to the conventional one. Also, both SAR controllers were evaluated using D-FF or HL-FF.

In Chapter 6, three different realizations of an 8-bit SA-ADC with low power, moderate speed, and moderate resolution for biomedical (low-frequency) applications were presented. They were implemented using the same S/H circuit which is based on a sampling transistor with dummy switch, the choice of static or dynamic comparator, the choice of conventional or clock gated SAR, and the same binary weighted capacitor array DAC. In addition to that, the SAR controller was implemented using D-FF or hybrid latch-FF. They have been designed using 90nm CMOS technology. It was worth to note that the structure's choice of each building blocks in the SA-ADC is not the only way to achieve minimum power consumption, but the suitable type of the FF should be selected in order to save a great amount of power consumption. The best proposed low-power clock gated SA-ADC using D-FF realization achieves 200 nW of power consumption without additional calibration or analog circuits. This realization consisted of mostly digital circuits in

order to lower the power consumption. Furthermore, the reconstruction of the real EEG signal was realized and it was consistent with the input real EEG signal waveform. Hence, the 8-bit digital codes of the proposed low-power clock gated SA-ADC using D-FF can be processed to diagnose the brain activities precisely.

7.2 Future Work

As a matter of fact, nothing is the best and nothing is the final. The continuous research explores new ideas and approaches that over perform the previous ones. In this section some suggestions are presented, which may facilitate further work.

The first step in the future work might be moving to medium-to-high frequency operation and propose a low power SA-ADC for high frequency applications. Furthermore, the design of the proposed SA-ADC can be improved in order to achieve further reduction in power consumption. One of the ideas is to design SA-ADC with monotonic capacitor switching procedure which proposed in [14] to reduce the switching energy and propose a compatible SAR logic structure.

One more attractive idea is to simulate the SA-ADC using DAC based SAR ADC architecture and charge re-distribution SAR ADC architecture in order to study the effect of the architecture on the power consumption.

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List of Published and Under Review Papers from the Master Thesis

1. S. A. Mahmoud, T. B. Nazzal, "Sample and Hold Circuits for Analog-to-Digital Converters," in UAE Graduate Students Research Conference (UAE GSRC 2015), pp. 223-224, Mar. 2015.

2. S. A. Mahmoud, T. B. Nazzal, "Sample and Hold Circuits for Low-Frequency Signals in Analog-to-Digital Converter," IEEE International Conference on Information and Communication Technology Research (ICTRC2015), pp. 33-36, 2015.

3. T. B. Nazzal, S. A. Mahmoud, "A 1-V 8-Bit Low-Power Clock Gated SAR ADC for Biomedical Applications" was accepted for Graduate Students Research Conference 2016 in UAE (UAE GSRC 2016).

4. T. B. Nazzal, S. A. Mahmoud, "On The Design of Low Power CMOS (SA- ADCs) for Biomedical Applications" was submitted for Circuits, Systems, and Signal Processing (CSSP).

5. T. B. Nazzal, S. A. Mahmoud, "A 200-nW 7.6-ENOB 10-KS/s SAR ADC in 90-nm CMOS for Portable Biomedical Applications" was submitted for Microelectronics.

6. A. A. Alhammadi, T. B. Nazzal, S. A. Mahmoud, "CMOS EEG Detection System with Analog Front-End Interleaved Architecture" was submitted for Analog Integrated Circuits and Signal Processing (ALOG).

7. T. B. Nazzal, S. A. Mahmoud, "A 1-V 8-Bit Ultra Low-Power Clock Gated SAR ADC without Additional Analog Circuits for Portable Biomedical Applications" to be submitted for Midwest Symposium on Circuits and Systems Conference 2016 (MWSCAS 2016).

8. T. B. Nazzal, S. A. Mahmoud, "Low-Power Bootstrapped Sample and Hold Circuit for Analog-to-Digital Converters" to be submitted for Midwest Symposium on Circuits and Systems Conference 2016 (MWSCAS 2016).

Appendix A

Derivations of the Dynamic Performance Metrics (SNR and ENOB) for Ideal ADC

$$SNR = 10 \log \frac{p_s}{p_q} \quad \text{(A.1)}$$

Where p_s: the signal power.

p_q: the noise power.

p_q = (noise amplitude)^2= (RMS quantization noise)^2

$$noise\ amplitude = \sqrt{\frac{1}{\Delta v} \int_{\frac{-\Delta v}{2}}^{\frac{\Delta v}{2}} q^2 dq} = \sqrt{\frac{\Delta v^2}{12}} \quad \text{(A.2)}$$

$$p_q = \left(\sqrt{\frac{\Delta v^2}{12}}\right)^2 = \frac{\Delta v^2}{12} \quad \text{(A.3)}$$

p_s=(signal amplitude)^2

$$RMS\ signal = \frac{\Delta v \times 2^N}{2\sqrt{2}} \quad \text{(A.4)}$$

$$p_s = \left(\frac{\Delta v \times 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta v^2 \times 2^{2N}}{8} \quad \text{(A.5)}$$

$$SNR = 10 \log\left(\frac{12 \times 2^{2N}}{8}\right) = 10N \times log 2^2 + 10 \log \frac{3}{2} = 6.02N + 1.76 \quad \text{(A.6)}$$

In the non-ideal ADCs the SNR is substituted with signal to noise and distortion ratio (SINAD).

Appendix B

Matlab Code for Static Performance Metrics (DNL and INL) Calculations

```
filename = sprintf('SAR%d/SAR%d Vout.txt', num, num);

x = dlmread(filename, '\t', 1, 0);

plot(x(:, 2));


if(from == -1)
    from = 1;
end

if(to == -1)
    to = length(x(:, 2));
end

y = x(from:to, 2)*256;
plot(y);

%%

minbin = min(y);
maxbin = max(y);

h = hist(y, minbin:maxbin);

ch = cumsum(h);

T = -cos(pi*ch/sum(h));

hlin = T(2:end) - T(1:end-1);

trunc=2;
hlin_trunc = hlin(1+trunc:end-trunc);

lsb = sum(hlin_trunc)/(length(hlin_trunc));
dnl = [0 hlin_trunc/lsb-1];

inl = cumsum(dnl);


[p, S] = polyfit(1:length(inl), inl, 1);
inl = inl - p(1)*[1:length(inl)]-p(2);

dnl = dnl/2;
```

```
inl = inl/2;


figure;
bar(dnl);

figure;
plot(inl);

filename = sprintf('sar%d', num);
save(filename, 'inl', 'dnl');
```

Appendix C

Netlist Code for Low-Power Clock Gated SA-ADC (Realization 3 using D-FF)

**********SAMPLE AND HOLD CIRCUIT**********

Connection

M1S Vin clks Vsampled 0 modn L=270n W=1080n

M2S Vsampled clksb Vsampled 0 modn L=270n W=540n

CS Vsampled 0 5pf

Clocks

vclks clks 0 PULSE (0 1 0 10n 10n 0.05m 0.1m)

vclksb clksb 0 PULSE (1 0 0 10n 10n 0.05m 0.1m)

Inputs

vinput Vin 0 sine (0.5 0.5 250)

*vinput Vin 0 DC 0V

*Veeg1 Vin 0 PWL value_scale_factor=0.25u time_scale_factor=1 repeat forever (FILE=beta.txt) endrepeat

*.lib C:\Users\SajaaN\Desktop\LTC\LTspiceIV\lib\cmp\standard.mos

```
********************************************************************************
******************
**********************************************COMPARATOR
CIRCUIT**************************************

***Connection***

M1C 3 Vsampled 2 0 modn L=90n W=180n
M2C 4 Vdac 2 0 modn L=90n W=180n
M3C 2 clkc 1 0 modn L=90n W=180n
M4C 1 Vbias 0 0 modn L=90n W=180n
M9C 3 clkc Vdd Vdd modp L=90n W=180n
M10C 4 clkc Vdd Vdd modp L=90n W=180n

M11C outn 3 0 0 modn L=90n W=990n
M5C outn outp 0 0 modn L=90n W=990n
M6C outp outn 0 0 modn L=90n W=990n
M12C outp 4 0 0 modn L=90n W=990n
M7C outn outp 7 Vdd modp L=90n W=990n
M8C outp outn 7 Vdd modp L=90n W=990n

M13C 7 clkcb Vdd Vdd modp L=90n W=180n

Mp1C Voutn outn Vdd Vdd modp L=90n W=180n
Mn1C Voutn outn 0 0 modn L=90n W=180n

Mp2C cmp outp Vdd Vdd modp L=90n W=180n
Mn2C cmp outp 0 0 modn L=90n W=180n
```

Clocks

vclkc clkc 0 PULSE (0 1 0 10n 10n 5u 10u)

Xin clkc clkcb Vdd inverter

*vclkcb clkcb 0 PULSE (1 0 10u 10u 10n 10n 5u 10u)

Inputs

*vinn Vinn 0 DC 0.25V

*vinp Vinp 0 sine (0.25 0.25 250)

Sources

*vdd Vdd 0 DC 1V

vbias Vbias 0 DC 0.55V

****
****

**********DAC
CIRCUIT**********

Connection

MuD Vdac S0 0 0 modn L=1170n W=1080n

M0nD node0 Q0 Vref 0 modn L=900n W=9000n

M0pD node0 Q0 0 Vref modp L=900n W=10800n

M1nD node1 Q1 Vref 0 modn L=900n W=9000n

M1pD node1 Q1 0 Vref modp L=900n W=10800n

M2nD node2 Q2 Vref 0 modn L=900n W=9000n

M2pD node2 Q2 0 Vref modp L=900n W=10800n

M3nD node3 Q3 Vref 0 modn L=900n W=9000n

M3pD node3 Q3 0 Vref modp L=900n W=10800n

M4nD node4 Q4 Vref 0 modn L=900n W=9000n

M4pD node4 Q4 0 Vref modp L=900n W=10800n

M5nD node5 Q5 Vref 0 modn L=900n W=9000n

M5pD node5 Q5 0 Vref modp L=900n W=10800n

M6nD node6 Q6 Vref 0 modn L=900n W=9000n

M6pD node6 Q6 0 Vref modp L=900n W=10800n

M7nD node7 Q7 Vref 0 modn L=900n W=9000n

M7pD node7 Q7 0 Vref modp L=900n W=10800n

Cu Vdac 0 50fF IC=0

C0 Vdac node0 50fF IC=0

C1 Vdac node1 100fF IC=0

C2 Vdac node2 200fF IC=0

C3 Vdac node3 400fF IC=0

C4 Vdac node4 800fF IC=0

C5 Vdac node5 1600fF IC=0

C6 Vdac node6 3200fF IC=0

C7 Vdac node7 6400fF IC=0

Clocks

vS0 S0 0 PULSE (1 0 10u 10n 10n 0.09m 0.1m)

Inputs

*VD0 D0 0 DC 1V

*Pulse (0 1)

*VD1 D1 0 DC 1V

*Pulse (0 1)

*VD2 D2 0 DC 1V

*Pulse (0 1)

*VD3 D3 0 DC 1V

*Pulse (0 1)

*VD4 D4 0 DC 1V

*Pulse (0 1)

*VD5 D5 0 DC 1V

*Pulse (0 1)

*VD6 D6 0 DC 1V

*Pulse (0 1)

*VD7 D7 0 DC 1V

*Pulse (0 1)

Sources

```
vref Vref 0 DC 1V
*PULSE (0 1)

**********************************************************************************************
**********SAR REGISTER CIRCUIT**********

***Connection***

*two input nand
.SUBCKT nand21 innand1 innand2 outnand Vdd

*vdd Vdd 0 DC 1V

Mpnand1 outnand innand1 Vdd Vdd modp L=180n W=360n
Mpnand2 outnand innand2 Vdd Vdd modp L=180n W=360n
Mnnand1 outnand innand1 1 0 modn L=180n W=360n
Mnnand2 1 innand2 0 0 modn L=180n W=360n

.ENDS nand21
***

*three input nand
.SUBCKT nand31 innand1 innand2 innand3 outnand Vdd

*vdd Vdd 0 DC 1V

Mpnand1 outnand innand1 Vdd Vdd modp L=180n W=360n
```

```
Mpnand2 outnand innand2 Vdd Vdd modp L=180n W=360n
Mpnand3 outnand innand3 Vdd Vdd modp L=180n W=360n
Mnnand1 outnand innand1 1 0 modn L=180n W=360n
Mnnand2 1 innand2 2 0 modn L=180n W=360n
Mnnand3 2 innand3 0 0 modn L=180n W=360n

.ENDS nand31
***

*D-flip flop
.SUBCKT dff clk Din reset Q Qb Vdd

Xnand1 out4 out2 out1 Vdd nand21

Xnand2 out1 clk reset out2 Vdd nand31

Xnand3 out2 clk out4 out3 Vdd nand31

Xnand4 out3 Din reset out4 Vdd nand31

Xnand5 out2 Qb Q Vdd nand21

Xnand6 Q out3 reset Qb Vdd nand31

.ENDS dff
***

*inverter0
```

```
.SUBCKT inverter0 ininv outinv Vdd

*vdd Vdd 0 DC 1V

Mpinv outinv ininv Vdd Vdd modp L=3690n W=180n
Mninv outinv ininv 0 0 modn L=3690n W=180n

.ENDS inverter0
***

*inverter

.SUBCKT inverter ininv outinv Vdd

*vdd Vdd 0 DC 1V

Mpinv outinv ininv Vdd Vdd modp L=180n W=360n
Mninv outinv ininv 0 0 modn L=180n W=360n

.ENDS inverter
***
*inverteri

.SUBCKT inverteri ininv outinv Vdd

*vdd Vdd 0 DC 1V

Mpinv outinv ininv Vdd Vdd modp L=90n W=180n
Mninv outinv ininv 0 0 modn L=90n W=180n
```

```
.ENDS inverteri
***


*two input and
.SUBCKT and21 innand1 innand2 outand Vdd

*vdd Vdd 0 DC 1V

Mpnand1 outnand innand1 Vdd Vdd modp L=180n W=360n
Mpnand2 outnand innand2 Vdd Vdd modp L=180n W=360n
Mnnand1 outnand innand1 1 0 modn L=180n W=360n
Mnnand2 1 innand2 0 0 modn L=180n W=360n

Xinvertern outnand outand Vdd inverter

.ENDS and21
***

*controller1
.SUBCKT controller1 clk stopb eQ0 eQ0b ecmpb eQ1 eQ1b eQ2 clkg0 clkg1 cout1 Vdd

*vdd Vdd 0 DC 1V

M4 4 clk Vdd Vdd modp L=270n W=360n
M5 5 clk Vdd Vdd modp L=270n W=360n
M6 clkg0 clk Vdd Vdd modp L=270n W=360n
M7 7 clk Vdd Vdd modp L=270n W=360n
```

M8 clkg1 clk Vdd Vdd modp L=270n W=360n

M1 4 clk 0 0 modn L=360n W=180n

M2 5 stopb 4 0 modn L=360n W=180n

M3 7 eQ0b 5 0 modn L=360n W=180n

M01 1a eQ0 5 0 modn L=360n W=180n

M02 clkg0 ecmpb 1a 0 modn L=360n W=180n

M03 2a eQ0b 5 0 modn L=360n W=180n

M04 clkg0 eQ1 2a 0 modn L=360n W=180n

M11 1b eQ1 7 0 modn L=360n W=180n

M12 clkg1 ecmpb 1b 0 modn L=360n W=180n

M13 2b eQ1b 7 0 modn L=360n W=180n

M14 clkg1 eQ2 2b 0 modn L=360n W=180n

Xinverter1 7 cout1 Vdd inverter

Xinverter2 clkg1 clkg11 Vdd inverter0

Xinverter3 clkg11 clkg1 Vdd inverter0

Xinverter4 clkg0 clkg00 Vdd inverter0

Xinverter5 clkg00 clkg0 Vdd inverter0

.ENDS controller1

***

*controller21

.SUBCKT controller21 clk eQ1b cout1 eQ2 eQ2b ecmpb eQ3 eQ3b eQ4 eQ4b eQ5 clkg2 clkg3 clkg4 cout2 Vdd

```
*vdd Vdd 0 DC 1V

M5 5 clk Vdd Vdd modp L=270n W=360n
M6 clkg2 clk Vdd Vdd modp L=270n W=360n
M7 7 clk Vdd Vdd modp L=270n W=360n
M8 clkg3 clk Vdd Vdd modp L=270n W=360n
M9 9 clk Vdd Vdd modp L=270n W=360n
M10 clkg4 clk Vdd Vdd modp L=270n W=360n

M1 a cout1 0 0 modn L=360n W=180n
M2 5 eQ1b a 0 modn L=360n W=180n
M3 7 eQ2b 5 0 modn L=360n W=180n
M4 9 eQ3b 7 0 modn L=360n W=180n

M21 1a eQ2 5 0 modn L=360n W=180n
M22 clkg2 ecmpb 1a 0 modn L=360n W=180n
M23 2a eQ2b 5 0 modn L=360n W=180n
M24 clkg2 eQ3 2a 0 modn L=360n W=180n

M31 1b eQ3 7 0 modn L=360n W=180n
M32 clkg3 ecmpb 1b 0 modn L=360n W=180n
M33 2b eQ3b 7 0 modn L=360n W=180n
M34 clkg3 eQ4 2b 0 modn L=360n W=180n

M41 1c eQ4 9 0 modn L=360n W=180n
M42 clkg4 ecmpb 1c 0 modn L=360n W=180n
M43 2c eQ4b 9 0 modn L=360n W=180n
M44 clkg4 eQ5 2c 0 modn L=360n W=180n
```

```
Xinverter1 9 cout2 Vdd inverter
Xinverter2 clkg4 clkg44 Vdd inverter0
Xinverter3 clkg44 clkg4 Vdd inverter0
Xinverter4 clkg3 clkg33 Vdd inverter0
Xinverter5 clkg33 clkg3 Vdd inverter0
Xinverter6 clkg2 clkg22 Vdd inverter0
Xinverter7 clkg22 clkg2 Vdd inverter0

.ENDS controller21
***

*controller22
.SUBCKT controller22 clk eQ4b cout2 eQ5 eQ5b ecmpb eQ6 eQ6b eQ7 clkg5 clkg6 clkg7 Vdd

*vdd Vdd 0 DC 1V

M5 5 clk Vdd Vdd modp L=270n W=360n
M6 clkg5 clk Vdd Vdd modp L=270n W=360n
M7 7 clk Vdd Vdd modp L=270n W=360n
M8 clkg6 clk Vdd Vdd modp L=270n W=360n
M9 9 clk Vdd Vdd modp L=270n W=360n
M10 clkg7 clk Vdd Vdd modp L=270n W=360n

M1 a cout2 0 0 modn L=360n W=180n
M2 5 eQ4b a 0 modn L=360n W=180n
M3 7 eQ5b 5 0 modn L=360n W=180n
M4 9 eQ6b 7 0 modn L=360n W=180n

M21 1a eQ5 5 0 modn L=360n W=180n
```

```
M22 clkg5 ecmpb 1a 0 modn L=360n W=180n
M23 2a eQ5b 5 0 modn L=360n W=180n
M24 clkg5 eQ6 2a 0 modn L=360n W=180n

M31 1b eQ6 7 0 modn L=360n W=180n
M32 clkg6 ecmpb 1b 0 modn L=360n W=180n
M33 2b eQ6b 7 0 modn L=360n W=180n
M34 clkg6 eQ7 2b 0 modn L=360n W=180n

M41 1c eQ7 9 0 modn L=360n W=180n
M42 clkg7 ecmpb 1c 0 modn L=360n W=180n

Xinverter2 clkg7 clkg77 Vdd inverter0
Xinverter3 clkg77 clkg7 Vdd inverter0
Xinverter4 clkg6 clkg66 Vdd inverter0
Xinverter5 clkg66 clkg6 Vdd inverter0
Xinverter6 clkg5 clkg55 Vdd inverter0
Xinverter7 clkg55 clkg5 Vdd inverter0

.ENDS controller22
***

*FF0
XFF0 clkg0 D0 reset Q0 Q0b Vdd dff
Vdq0 D0 Q0b DC 0V

*FF1
XFF1 clkg1 D1 reset Q1 Q1b Vdd dff
Vdq1 D1 Q1b DC 0V
```

Xcontroller1 clkm stopbm Q0 Q0b cmpb Q1 Q1b Q2 clkg0 clkg1 cout1m Vdd controller1

*FF2

XFF2 clkg2 D2 reset Q2 Q2b Vdd dff

Vdq2 D2 Q2b DC 0V

*FF3

XFF3 clkg3 D3 reset Q3 Q3b Vdd dff

Vdq3 D3 Q3b DC 0V

*FF4

XFF4 clkg4 D4 reset Q4 Q4b Vdd dff

Vdq4 D4 Q4b DC 0V

Xcontroller21 clkm Q1b cout1m Q2 Q2b cmpb Q3 Q3b Q4 Q4b Q5 clkg2 clkg3 clkg4 cout2m Vdd controller21

*FF5

XFF5 clkg5 D5 reset Q5 Q5b Vdd dff

Vdq5 D5 Q5b DC 0V

*FF6

XFF6 clkg6 D6 reset Q6 Q6b Vdd dff

Vdq6 D6 Q6b DC 0V

*FF7

XFF7 clkg7 D7 reset Q7 Q7b Vdd dff

Vdq7 D7 Q7b DC 0V

```
Xcontroller22 clkm Q4b cout2m Q5 Q5b cmpb Q6 Q6b Q7 clkg5 clkg6 clkg77 Vdd controller22

***Clocks***

vreset reset 0 PULSE (0 1 5u 10n 10n 90u 0.1m)
vreset7 reset7 0 PULSE (0 1 0 10n 10n 0.09m 0.1m)

Vstopbm stopbm 0 1V
*PULSE (0 1 0.01u 10n 10n 0.097m 0.1m)

vclk clkm 0 PULSE (0 1 5.7u 10n 10n 5u 10u)
Vclk70 clk70 0 PULSE (1 0 5.7u 10n 10n 5u 100u)

Xclk clkg77 clk70 clkg7 Vdd and21

***Inputs***

*Vcmp cmp 0 DC 0V
Xinverter cmp cmpb Vdd inverteri

***Sources***

vdd Vdd 0 DC 1V

********************************************************************************
******************************
**********************************************DAC RECONSTRUCTION
CIRCUIT**********************************************
```

MuDr Vdacr S0r 0 0 modn L=1170n W=1080n

M0nDr node0r Q0 Vref 0 modn L=900n W=9000n

M0pDr node0r Q0 0 Vref modp L=900n W=10800n

M1nDr node1r Q1 Vref 0 modn L=900n W=9000n

M1pDr node1r Q1 0 Vref modp L=900n W=10800n

M2nDr node2r Q2 Vref 0 modn L=900n W=9000n

M2pDr node2r Q2 0 Vref modp L=900n W=10800n

M3nDr node3r Q3 Vref 0 modn L=900n W=9000n

M3pDr node3r Q3 0 Vref modp L=900n W=10800n

M4nDr node4r Q4 Vref 0 modn L=900n W=9000n

M4pDr node4r Q4 0 Vref modp L=900n W=10800n

M5nDr node5r Q5 Vref 0 modn L=900n W=9000n

M5pDr node5r Q5 0 Vref modp L=900n W=10800n

M6nDr node6r Q6 Vref 0 modn L=900n W=9000n

M6pDr node6r Q6 0 Vref modp L=900n W=10800n

M7nDr node7r Q7 Vref 0 modn L=900n W=9000n

M7pDr node7r Q7 0 Vref modp L=900n W=10800n

Cur Vdacr 0 50fF IC=0

C0r Vdacr node0r 50fF IC=0

C1r Vdacr node1r 100fF IC=0

C2r Vdacr node2r 200fF IC=0

C3r Vdacr node3r 400fF IC=0

C4r Vdacr node4r 800fF IC=0

C5r Vdacr node5r 1600fF IC=0

C6r Vdacr node6r 3200fF IC=0

C7r Vdacr node7r 6400fF IC=0

Clocks

vS0r S0r 0 PULSE (1 0 10u 10n 10n 0.09m 0.1m)

****
****

**********RECONSTRUCTION
SAMPLER**********

M1Sr Vdacr clksr Vdacrsampled 0 modn L=0.25u W=1u

M2Sr Vdacrsampled clksbr Vdacrsampled 0 modn L=0.25u W=0.5u

CSr Vdacrsampled 0 0.007pf

Clocks

vclksr clksr 0 PULSE (-0.7 1.5 180u 10n 10n 10u 0.1m)

vclksbr clksbr 0 PULSE (-0.7 1.5 90u 10n 10n 90u 0.1m)

*vclksr clksr 0 PULSE (0 1 0 10n 10n 0.05m 0.1m)

```
*vclksbr clksbr 0 PULSE (1 0 0 10n 10n 0.05m 0.1m)

**********************************LOW PASS
FILTER**************************************

e1l vout22 0 Vdacrsampled 0 1

R1l vout22 C1in 0.9K

R2l C1in C2in 0.9K

C1l C1in Vo 1uF

C2l C2in 0 0.35uF

e2l Vo 0 C2in 0 1

*********************************************************************************
******************

***********************************************MOSFET
MODELS*******************************************

.MODEL modn NMOS                        LEVEL   = 54

+          BINUNIT = 1          PARAMCHK= 1

+MOBMOD  = 2          RDSMOD  = 0          IGCMOD  = 0

+IGBMOD  = 0          CAPMOD  = 2          RGATEMOD= 0

+RBODYMOD= 0          TRNQSMOD= 0          ACNQSMOD= 0

+FNOIMOD = 1          TNOIMOD = 0          DIOMOD  = 1

+PERMOD  = 1          GEOMOD  = 0          EPSROX  = 3.9

+TOXE    = 2.8E-9       NGATE   = 1E20         RSH     = 7.5

+VTH0    = 0.1132772     K1      = 0.3020201     K2      = -0.1000081

+K3      = 1.001E-3      K3B     = 1.1392646     W0      = 1.001E-10

+LPE0    = 4.279228E-7   LPEB    = 3.322315E-8   DVT0    = 0.0118744

+DVT1    = 0.0305091     DVT2    = -2.845656E-5  DVTP0   = 0
```

+DVTP1 = 0 DVT0W = 0 DVT1W = 0

+DVT2W = -0.032 U0 = 485.3006766 UA = 1.950434E-15

+UB = 1.133994E-21 UC = -3.85186E-16 EU = 1.6388401

+VSAT = 7.201089E4 A0 = 1.7749808 AGS = 1.8250041

+B0 = -2.407235E-7 B1 = 0 KETA = 9.260569E-3

+A1 = 0 A2 = 1 WINT = 1.594168E-14

+LINT = 0 DWG = 8.175493E-9 DWB = 6.996022E-9

+VOFF = -1.344082E-3 NFACTOR = 1.2097665 ETA0 = 6.935862E-3

+ETAB = -1.42221E-3 DSUB = 0.1380789 CIT = 0

+CDSC = 2.4E-4 CDSCB = 0 CDSCD = 0

+PCLM = 1.0389842 PDIBLC1 = 0.9995331 PDIBLC2 = 0.01

+PDIBLCB = -1E-3 DROUT = 0.7469525 PSCBE1 = 7.95216E8

+PSCBE2 = 3E-6 PVAG = 3.081023E-3 DELTA = 9.493818E-3

+FPROUT = 2.007663E-5 RDSW = 353.0836308 RDSWMIN = 100

+RDW = 100 RDWMIN = 0 RSW = 100

+RSWMIN = 0 PRWG = 3 PRWB = -1E-3

+WR = 1 ALPHA0 = 0 ALPHA1 = 0

+BETA0 = 30 AGIDL = 0 BGIDL = 2.3E9

+CGIDL = 0.5 EGIDL = 0.8 XPART = 0.5

+CGSO = 3.1E-10 CGDO = 3.1E-10 CGBO = 1E-12

+CF = 0 CJS = 9.074861E-4 CJD = 9.074861E-4

+MJS = 0.4575932 MJD = 0.4575932 MJSWS = 0.4575932

+MJSWD = 0.4575932 CJSWS = 3.065074E-11 CJSWD = 3.065074E-11

+CJSWGS = 3.065074E-11 CJSWGD = 3.065074E-11 MJSWGS = 0.4575932

+MJSWGD = 0.4575932 PBSWS = 0.9923389

+PBSWD = 0.9923389 PBSWGS = 0.9923389 PBSWGD = 0.9923389

+TNOM = 27 PVTH0 = 7.302825E-5 PRDSW = 5.839325E-3

+PK2 = -1.122665E-3 WKETA = -0.0324687 LKETA = -0.019741

+PKETA = 4.851968E-3 PETA0 = 0 PVSAT = -148.7939847

```
+PU0    = 0.1459098     PUA    = -1E-18       PUB    = -1.51987E-20
*


.MODEL modp PMOS                        LEVEL   = 54
+          BINUNIT = 1          PARAMCHK= 1
+MOBMOD  = 2          RDSMOD  = 0          IGCMOD  = 0
+IGBMOD  = 0          CAPMOD  = 2          RGATEMOD= 0
+RBODYMOD= 0          TRNQSMOD= 0          ACNQSMOD= 0
+FNOIMOD = 1          TNOIMOD = 0          DIOMOD  = 1
+PERMOD  = 1          GEOMOD  = 0          EPSROX  = 3.9
+TOXE    = 2.8E-9      NGATE   = 1E20        RSH    = 7.9
+VTH0    = -0.0733208    K1     = 0.1821711     K2     = -1.810872E-3
+K3     = 3.5449173     K3B    = 10          W0     = 4.090756E-6
+LPE0    = 9.065404E-7   LPEB    = 3.005599E-7   DVT0    = 8.826159E-3
+DVT1    = 0.0266802     DVT2    = -6.109741E-5  DVTP0   = 0
+DVTP1   = 0           DVT0W   = 0           DVT1W   = 0
+DVT2W   = -0.032       U0     = 106.7690996   UA     = 1.720273E-15
+UB     = 1.770954E-22  UC     = -4.3757E-16   EU     = 1.5257692
+VSAT    = 1.471181E5    A0     = 2           AGS    = 0
+B0     = 2.5375E-7     B1     = 1E-7        KETA    = -0.0583176
+A1     = 0           A2     = 1           WINT    = -2.033811E-8
+LINT    = -2.025547E-8  DWG    = 1.989172E-12  DWB    = 4.540095E-12
+VOFF    = -2.548791E-5  NFACTOR = 1.0831381     ETA0   = 1.639851E-3
+ETAB    = -0.2         DSUB    = 0.9114354     CIT    = 0
+CDSC    = 2.4E-4       CDSCB   = 0           CDSCD   = 0
+PCLM    = 0.5090776     PDIBLC1 = 1           PDIBLC2 = 1.557269E-3
+PDIBLCB = -1E-3        DROUT   = 0.7494485     PSCBE1  = 7.960112E8
+PSCBE2  = 3E-6         PVAG    = 0.0507409     DELTA   = 0.03
+FPROUT  = 9.330108E-4   RDSW    = 1.407469E3     RDSWMIN = 100
```

+RDW = 100 RDWMIN = 0 RSW = 100

+RSWMIN = 0 PRWG = 0.1 PRWB = 0.1

+WR = 1 ALPHA0 = 0 ALPHA1 = 0

+BETA0 = 30 AGIDL = 0 BGIDL = 2.3E9

+CGIDL = 0.5 EGIDL = 0.8 XPART = 0.5

+CGSO = 3.2E-10 CGDO = 3.2E-10 CGBO = 1E-12

+CF = 0 CJS = 8.5E-4 CJD = 8.5E-4

+MJS = 0.309 MJD = 0.309 MJSWS = 0.033

+MJSWD = 0.033 CJSWS = 6.3E-11 CJSWD = 6.3E-11

+CJSWGS = 6.3E-11 CJSWGD = 6.3E-11 MJSWGS = 0.033

+MJSWGD = 0.033 PBSWS = 1

+PBSWD = 1 PBSWGS = 1 PBSWGD = 1

+TNOM = 27 PVTH0 = 5.145925E-4 PRDSW = 4.498705E-4

+PK2 = 6.850656E-4 WKETA = -8.000212E-3 LKETA = -0.0449768

+PKETA = 3.27593E-3 PETA0 = 0.0564108 PVSAT = -100

+PU0 = 1.0940866 PUA = -9.75453E-20 PUB = 1.73209E-21

****
****

**********SIMULATION
COMMANDS**********

.op

.probe

.tran 1000n 400m 0 1000n UIC

*.noise V(Vo) vinput dec 100 1 500

.backanno

.end