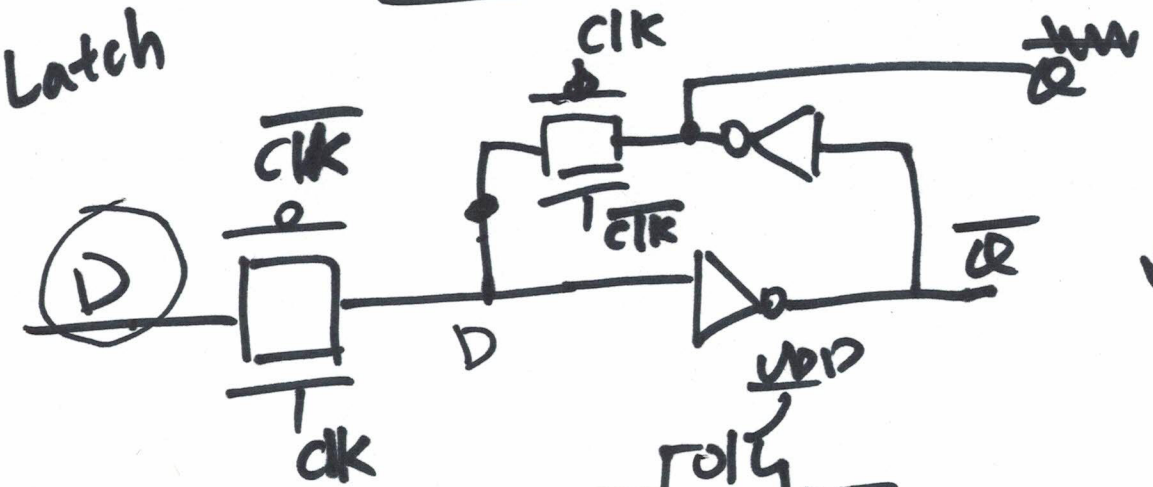
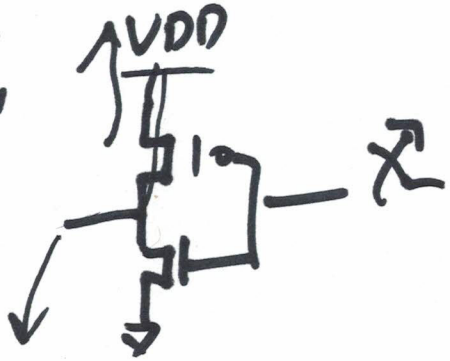
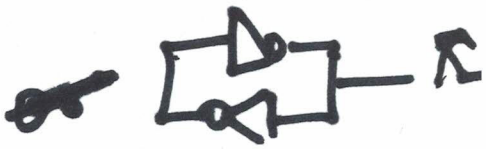
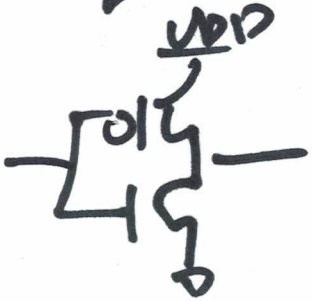
clocked Circuit

D Latch









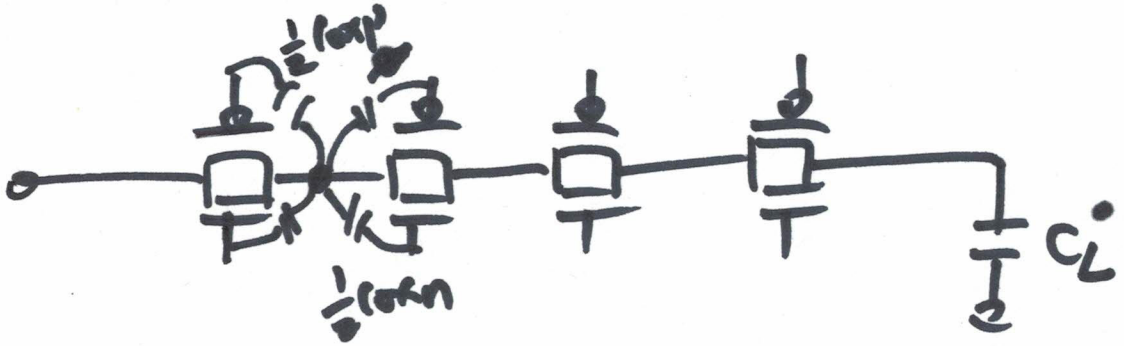
① D flip flop

② ↗ and 0, ~~Bypasses~~ samples Q Stores D

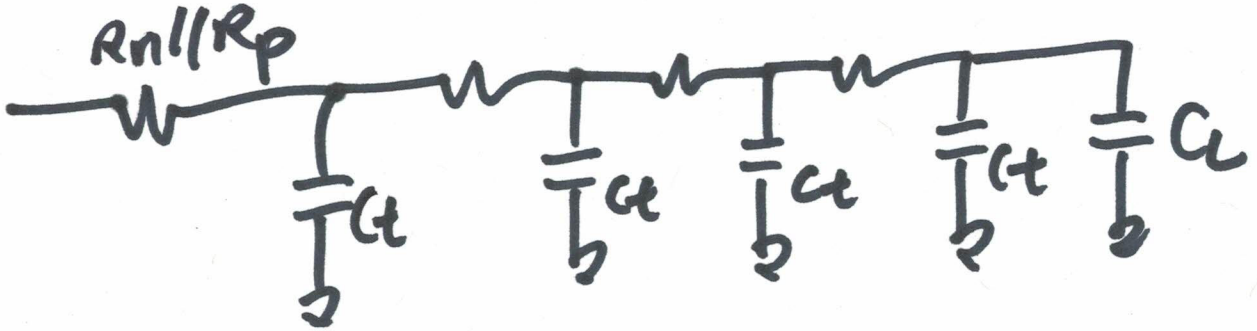
↘ and 1, updates Q

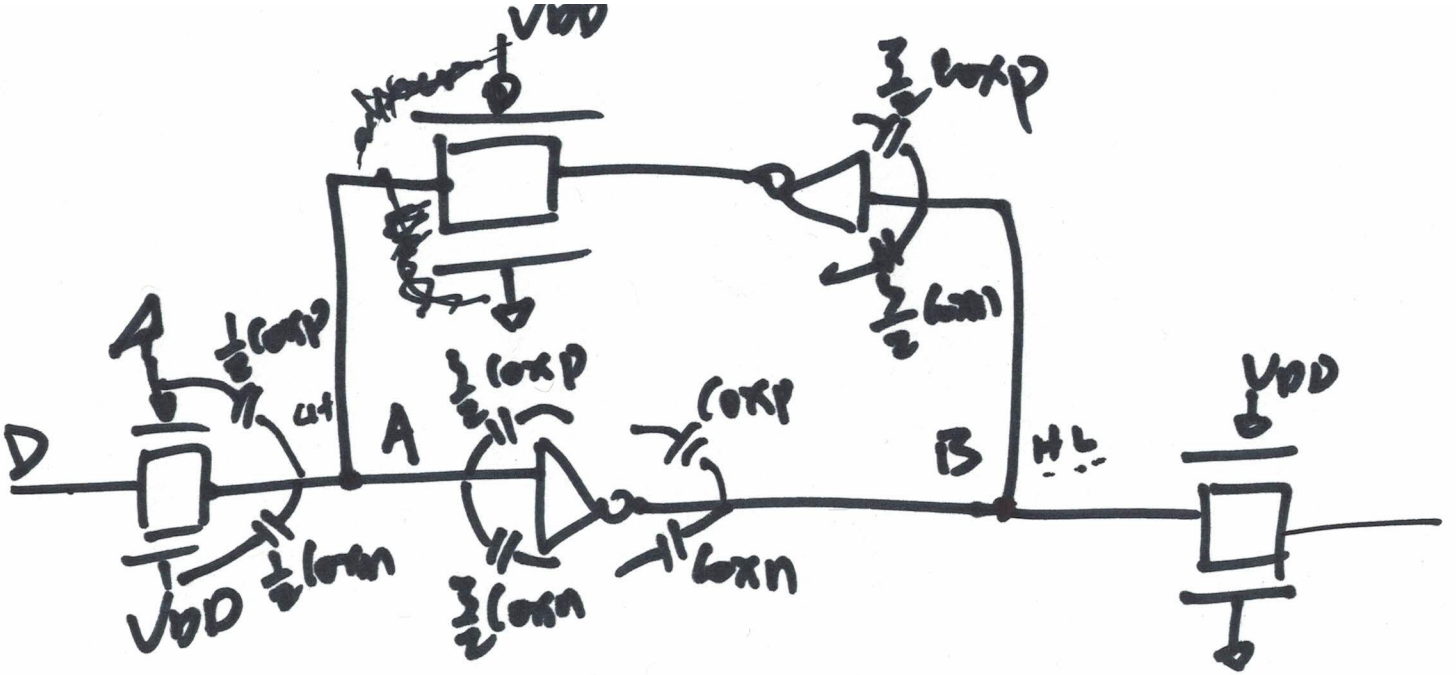
③ Asynchronous

①



$$C_{tot} = C_{ovn} + C_{ovp}$$





t_d: D→A: $C_A = 2(C_{oxn} + C_{oxp})$

A→B: $C_B = \frac{5}{2}(C_{oxn} + C_{oxp})$

D→B:

$$t_{PHL} = t_{PLH(D\to A)} + t_{PHL(A\to B)}$$
$$= 0.7(R_n \| R_p)\cdot C_A + 0.7 R_n \cdot C_B$$

$$t_{PLH} = t_{PHL(D\to B)} + t_{PLH(A\to B)}$$
$$= 0.7(R_n \| R_p)\cdot C_A + 0.7 \cdot R_p \cdot C_B$$

SRAM

Static RAm

etc cache

fast

expensive

DRAM

RAM

Card

Computer

cheaper

SRAM

SRAM

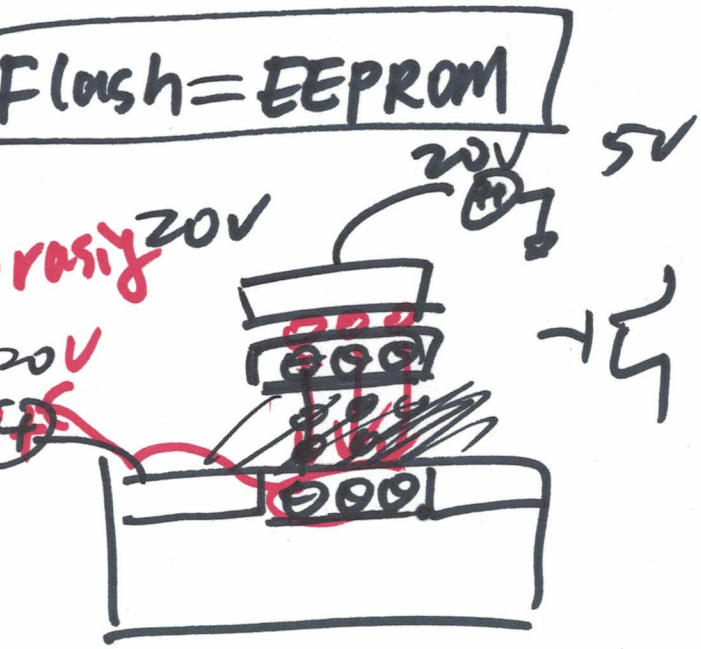
DRAM

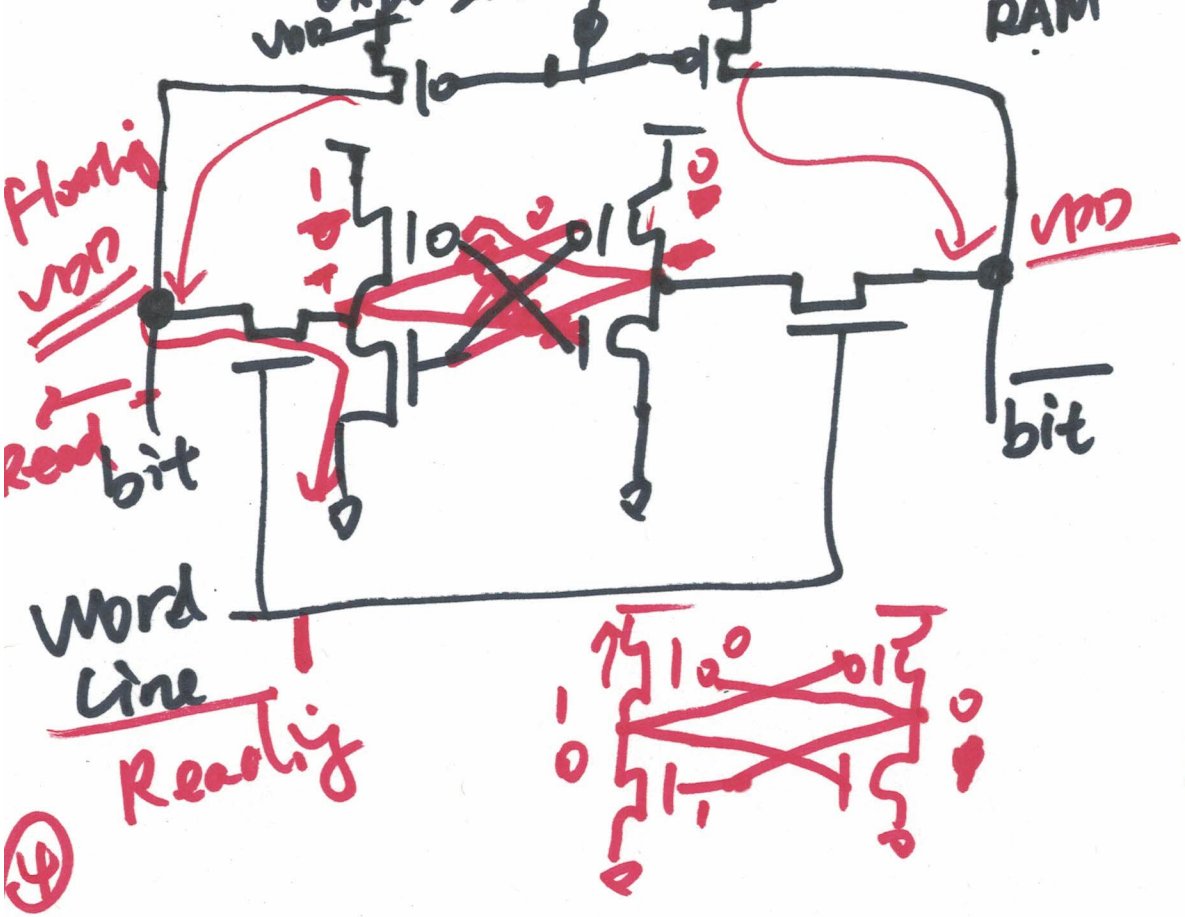
Synchronous

Dynamic

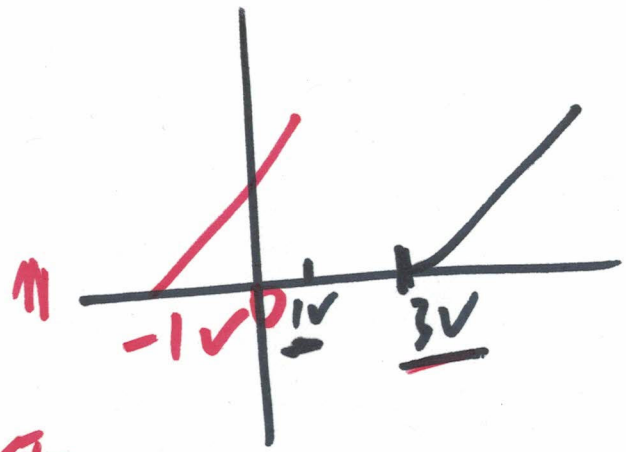
RAM

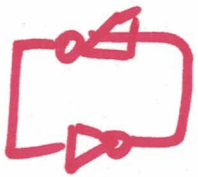
Flash=EEPROM





charge pump





(4)