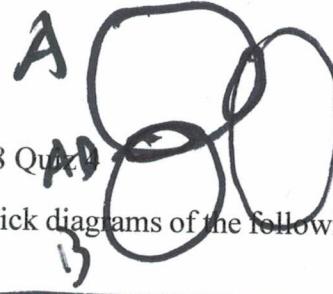


$$A = A \times 1$$

ENGR338 Quad

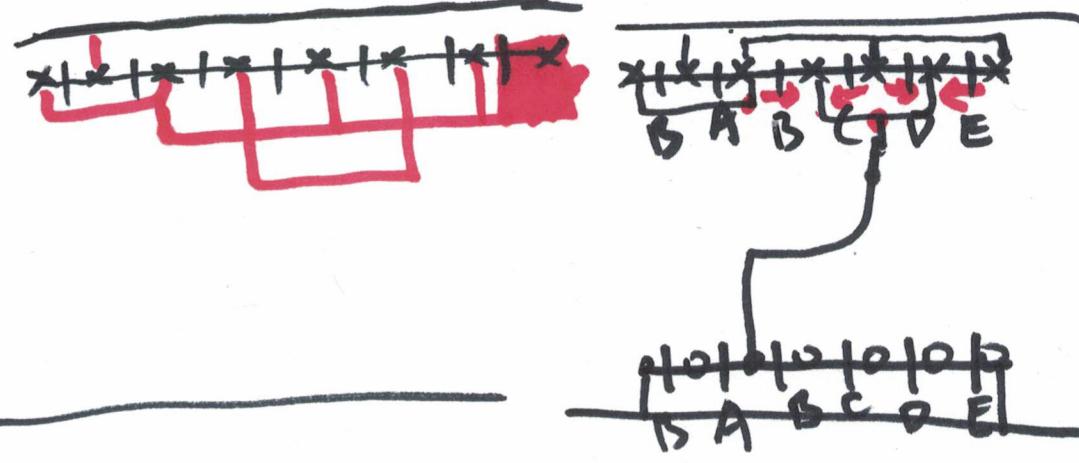
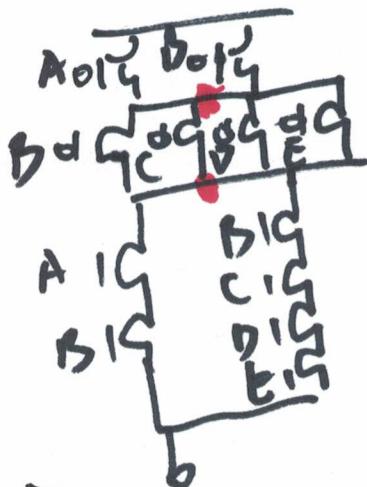


1. Draw the complex CMOS schematics and the stick diagrams of the following logic expressions. (25 points for each)

a. $\overline{(AB + A + ABD + CDE + ABCD)}B$

b. $\overline{ABC + DEF}$

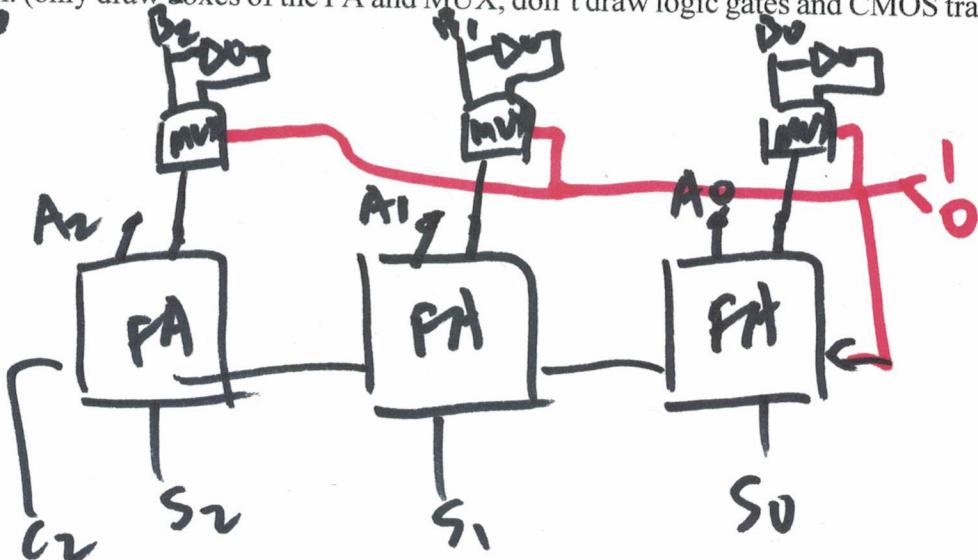
$$\begin{aligned} &= \overline{(A(1+B+BD+BCD) + (CDE)) \cdot B} \\ &= \overline{AB + BCDE} \end{aligned}$$

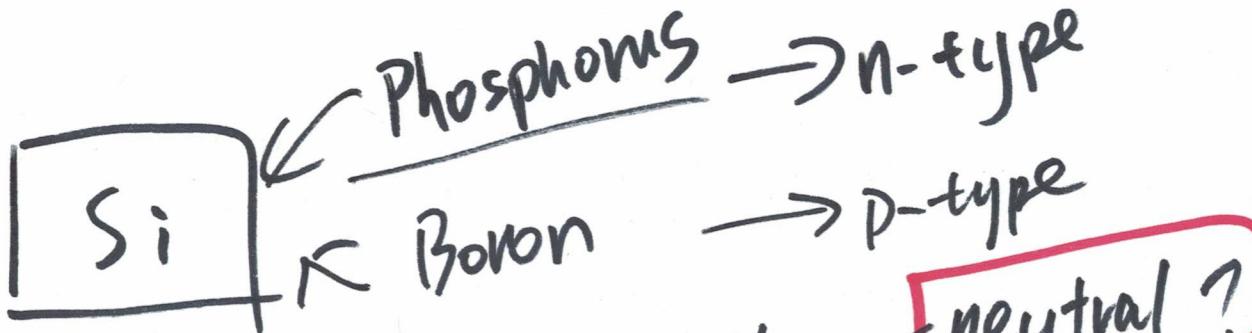


A $\overline{011} \overline{101} \overline{011}$
B $\overline{011} \overline{001} \overline{011}$
C $\overline{011} \overline{011} \overline{011}$
D $\overline{011} \overline{001} \overline{001}$
E $\overline{011} \overline{011} \overline{011}$

D $\overline{011} \overline{001} \overline{001}$
A $\overline{011} \overline{011} \overline{011}$
B $\overline{011} \overline{001} \overline{001}$
C $\overline{011} \overline{011} \overline{011}$
D $\overline{011} \overline{001} \overline{001}$
E $\overline{011} \overline{011} \overline{011}$
F $\overline{011} \overline{001} \overline{001}$

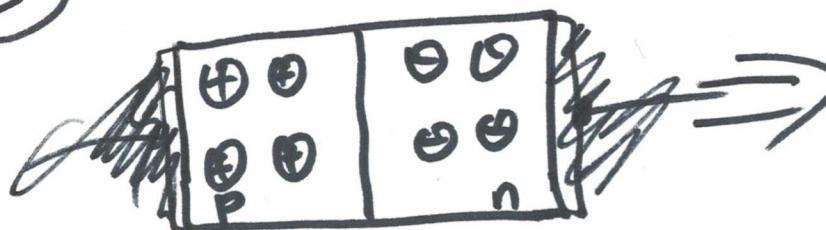
2. Draw the block schematic of a 3-bit adder/subtractor. Use MUXes and control bits to control the operation. (only draw boxes of the FA and MUX, don't draw logic gates and CMOS transistors). (50 points)



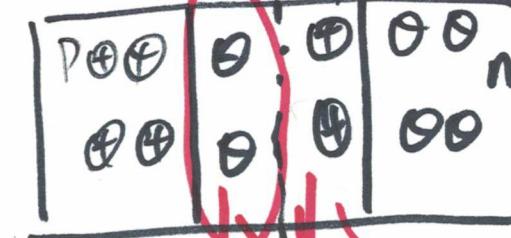


① Doped Si \rightarrow electrically

②



neutral?
negative
positive
 \rightarrow negatively charged



\rightarrow negatively charged

positively charged

depletion area/region



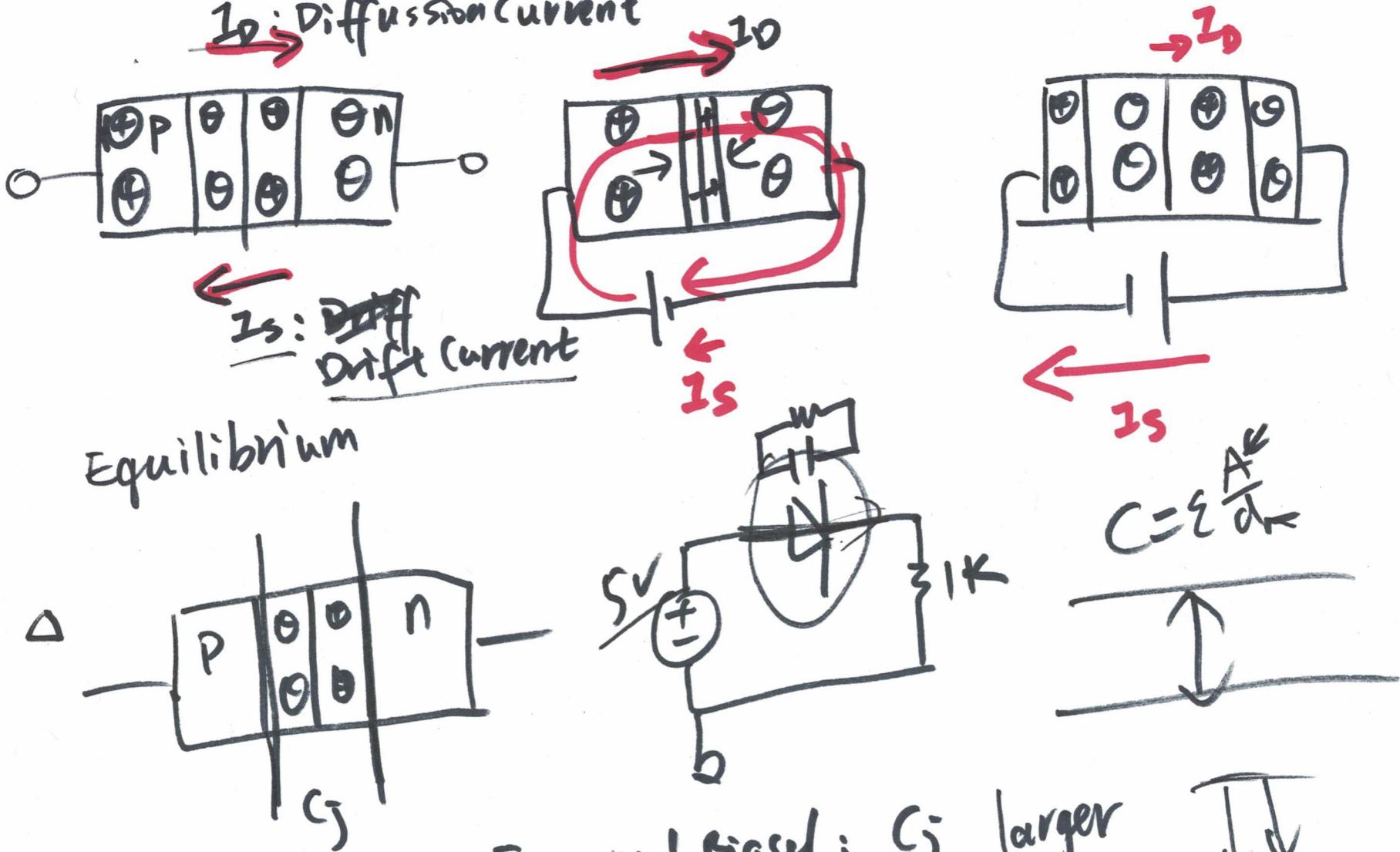
$\Leftarrow \Rightarrow V_b$: built-in voltage

$0.6 - 0.9 \text{ V}$ OR barrier voltage

Forward Biased

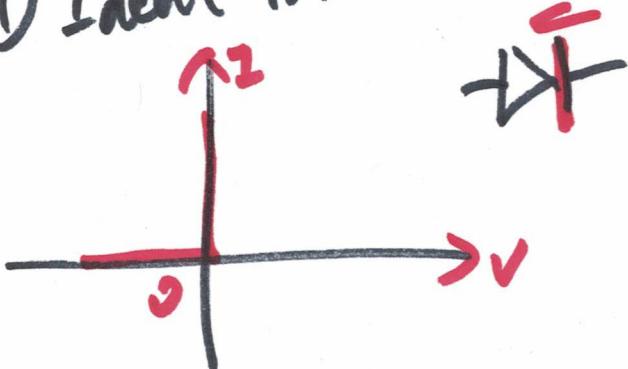
reverse Biased

③

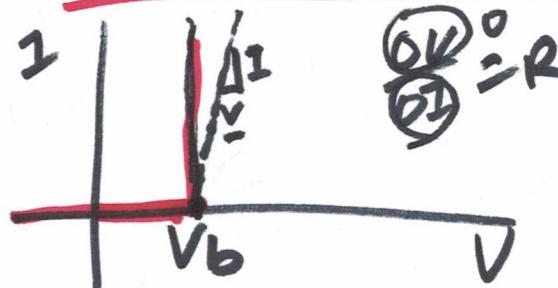


Forward Biased: $C_J 1$ larger
 Reverse Biased: $C_J 2$ smaller

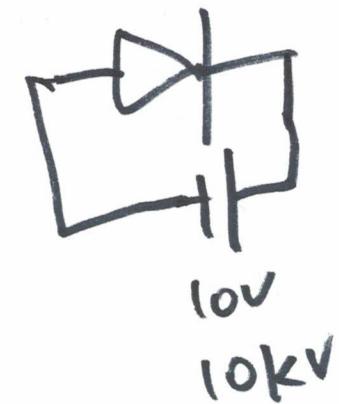
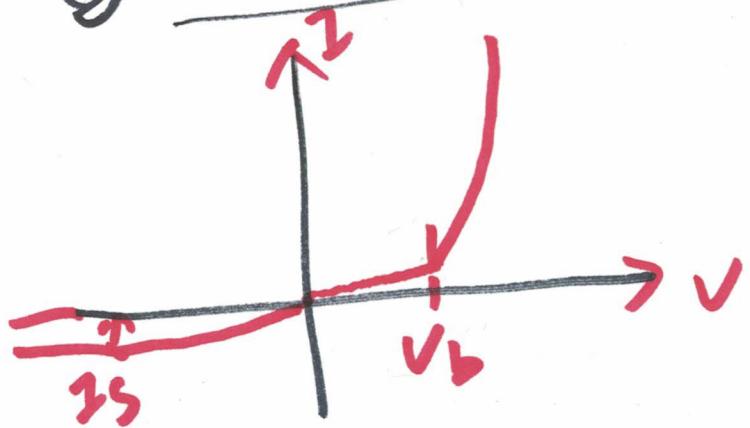
① Ideal Diode:



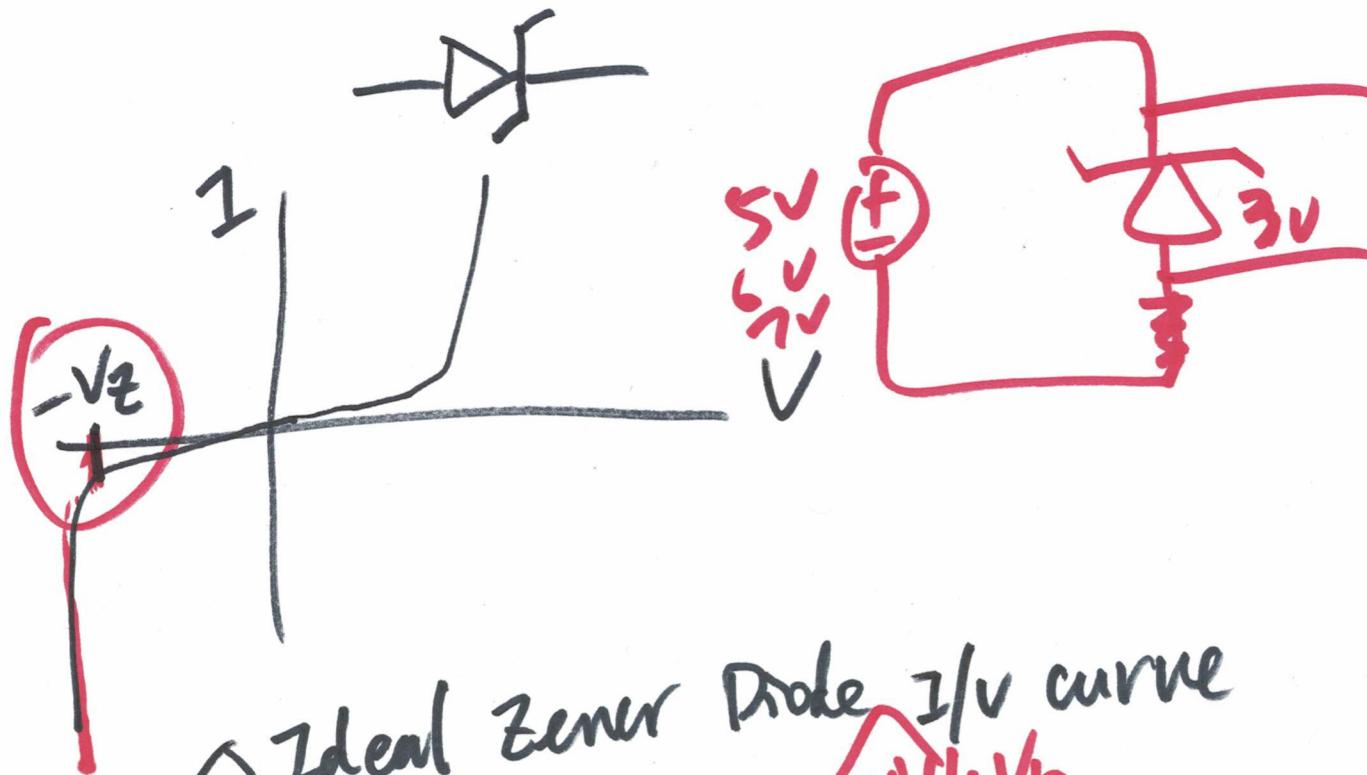
② Ideal Diode with V_b



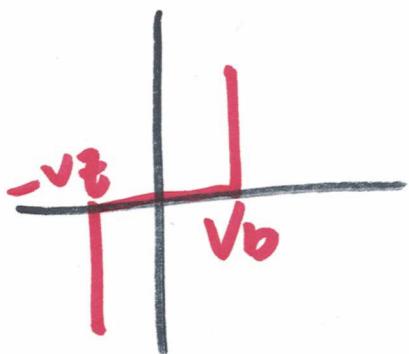
③ real diode, no reverse breakdown



Zener Diodes → used for stabilizing voltages



Ideal Zener Diode I/V curve
with V_b



AD1/Slick

DAC (superposition/Thevenin), state Diagrams

INL/DNLS

Adder/Subtractor