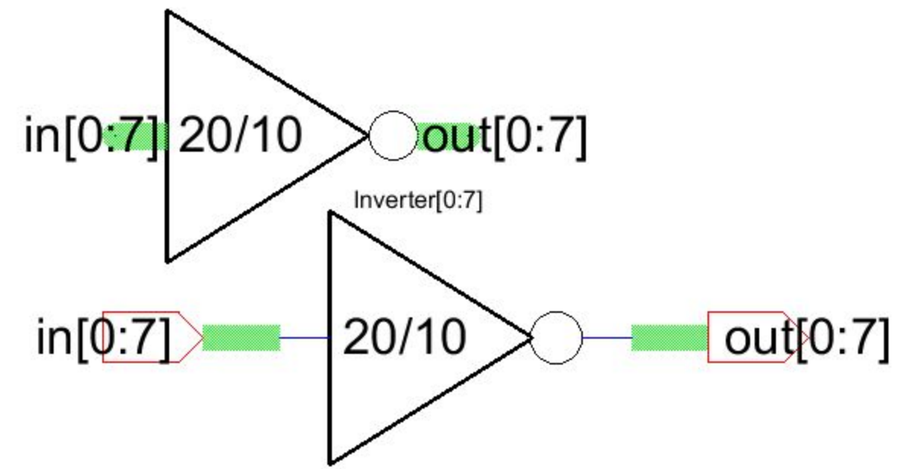
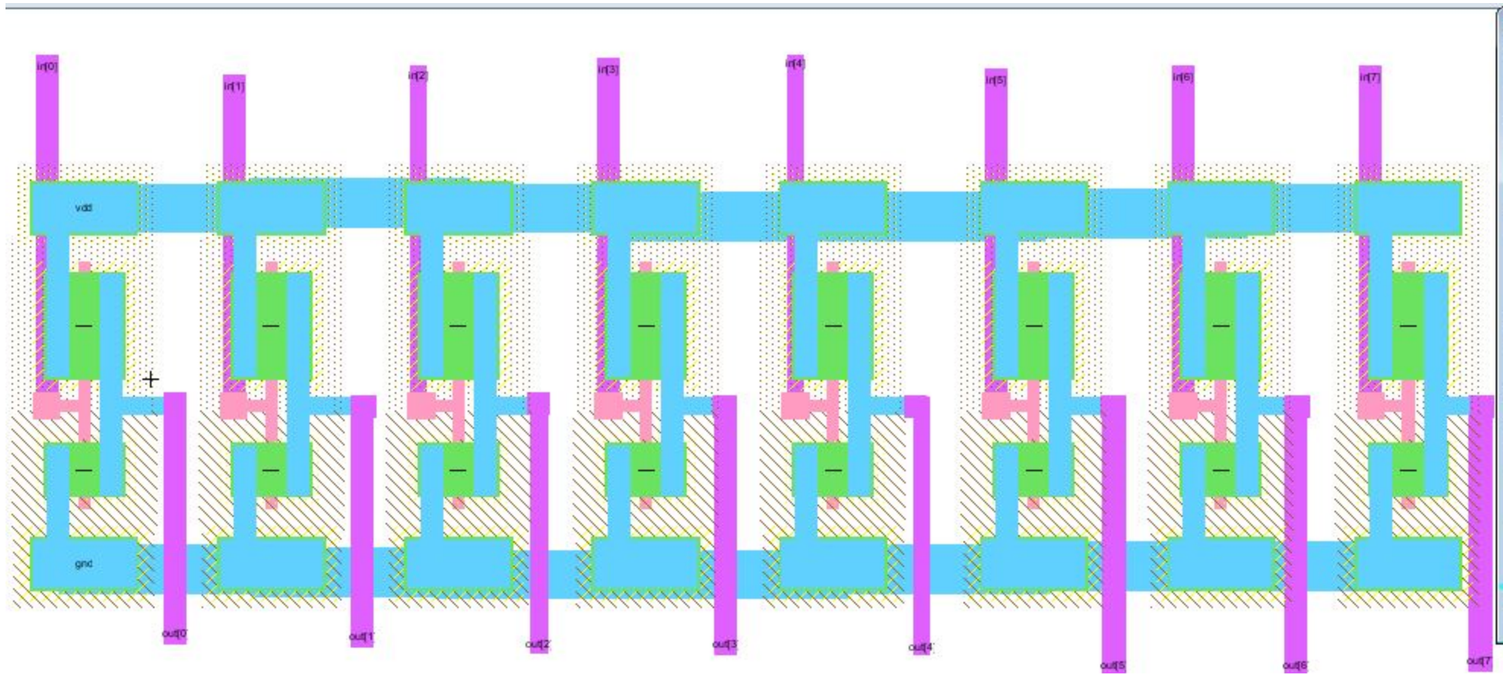
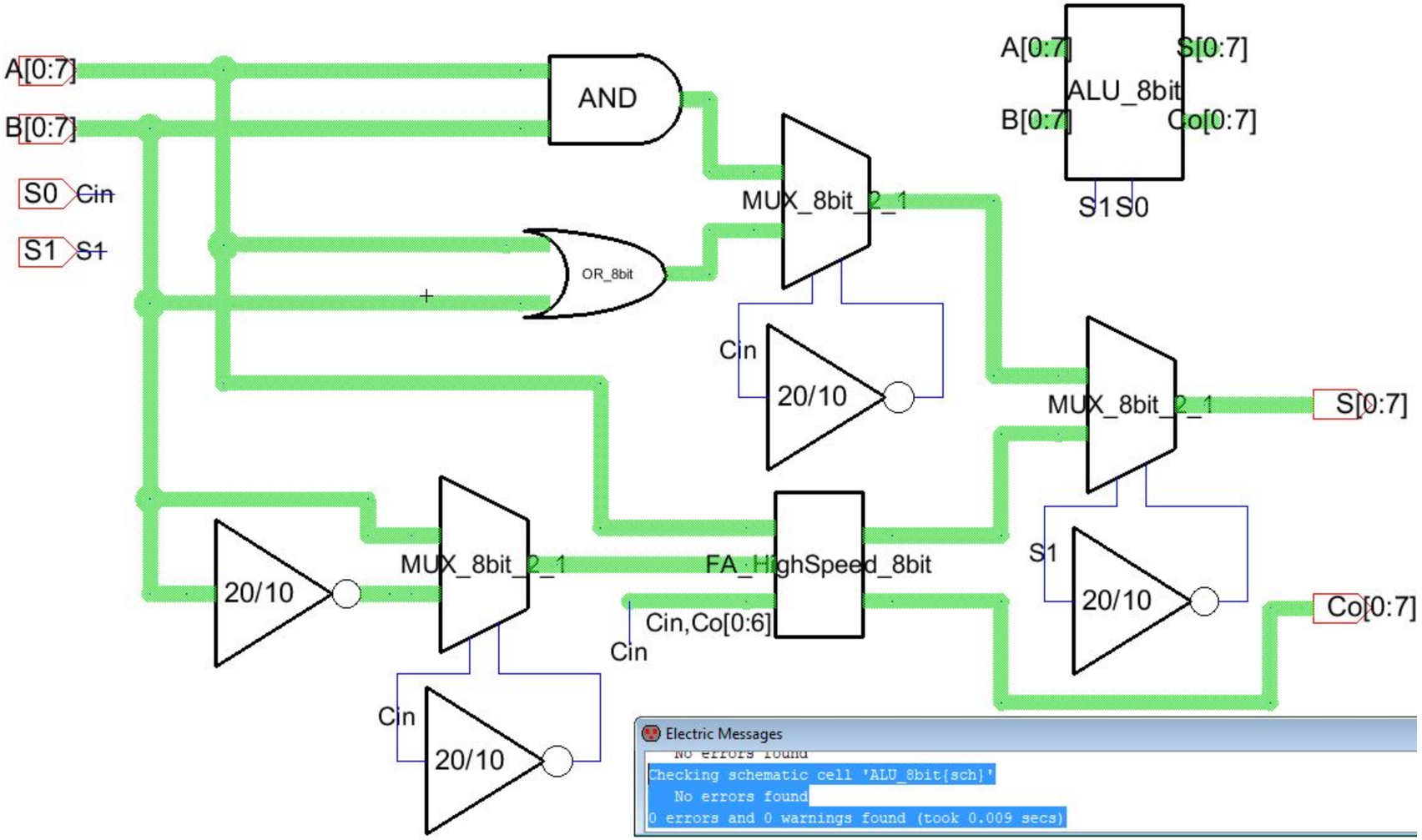


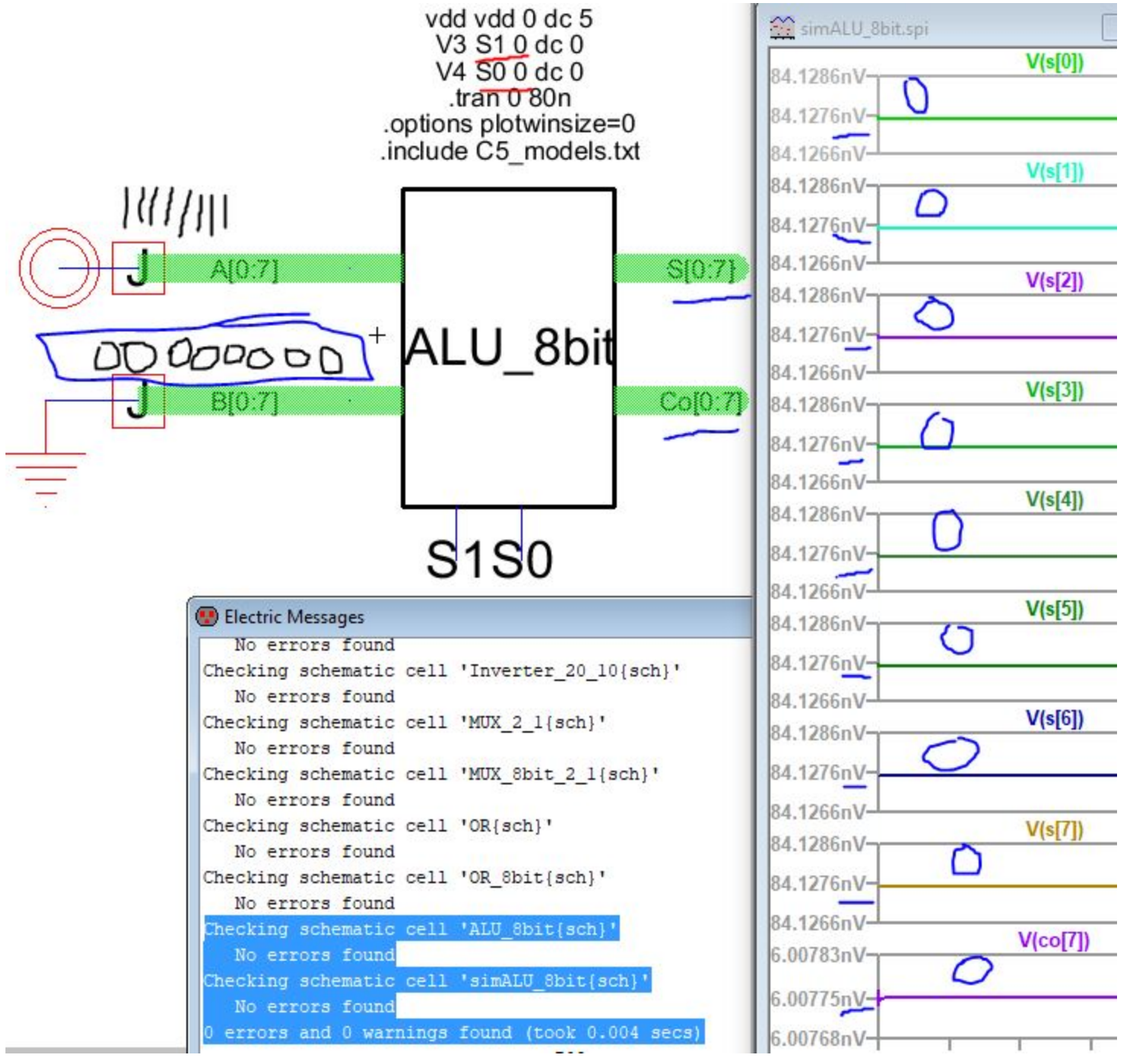

```
Checking schematic cell 'Inverter_Short_8bit_20_10{sch}'
   No errors found
0 errors and 0 warnings found (took 0.0 secs)
```

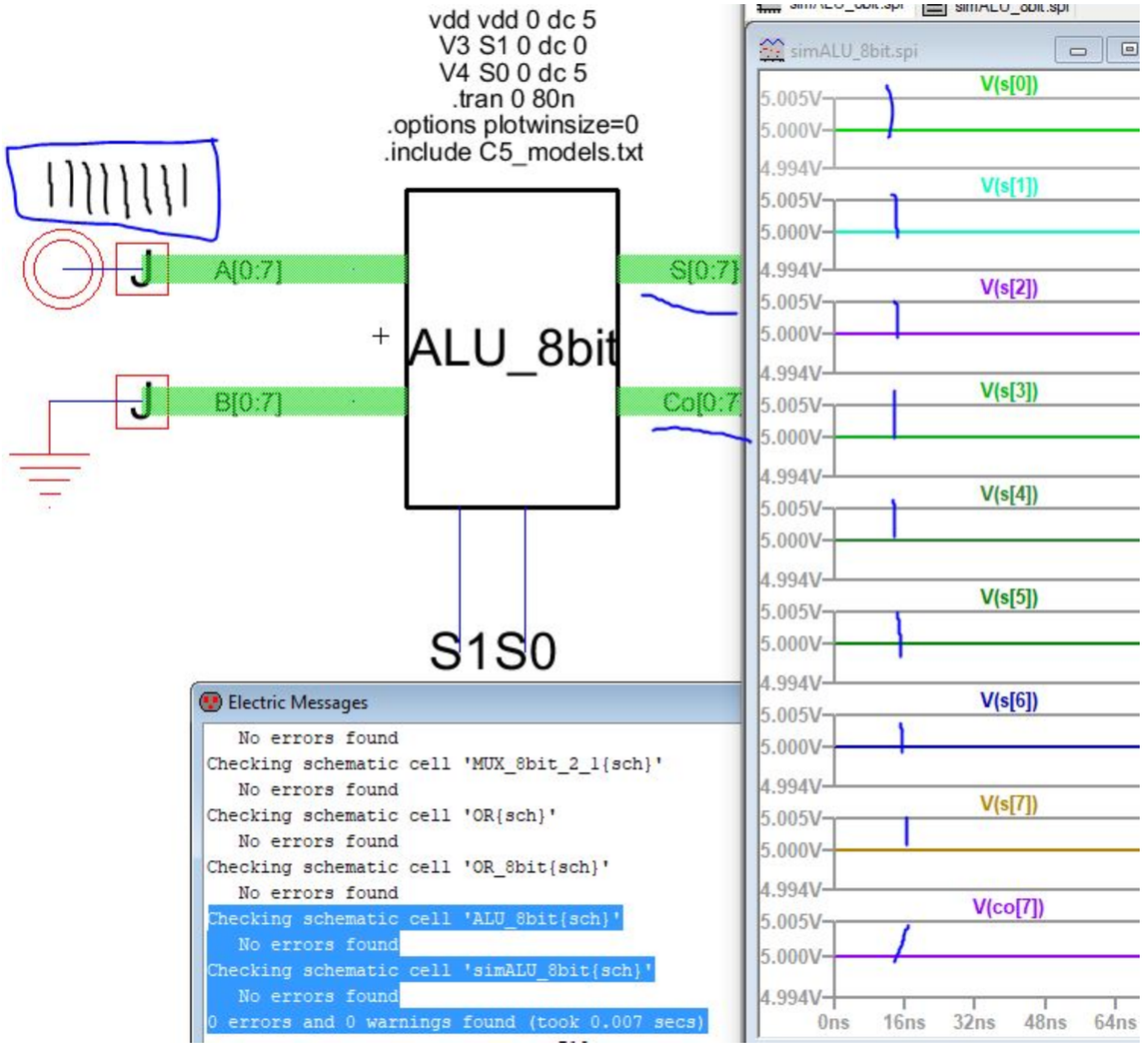


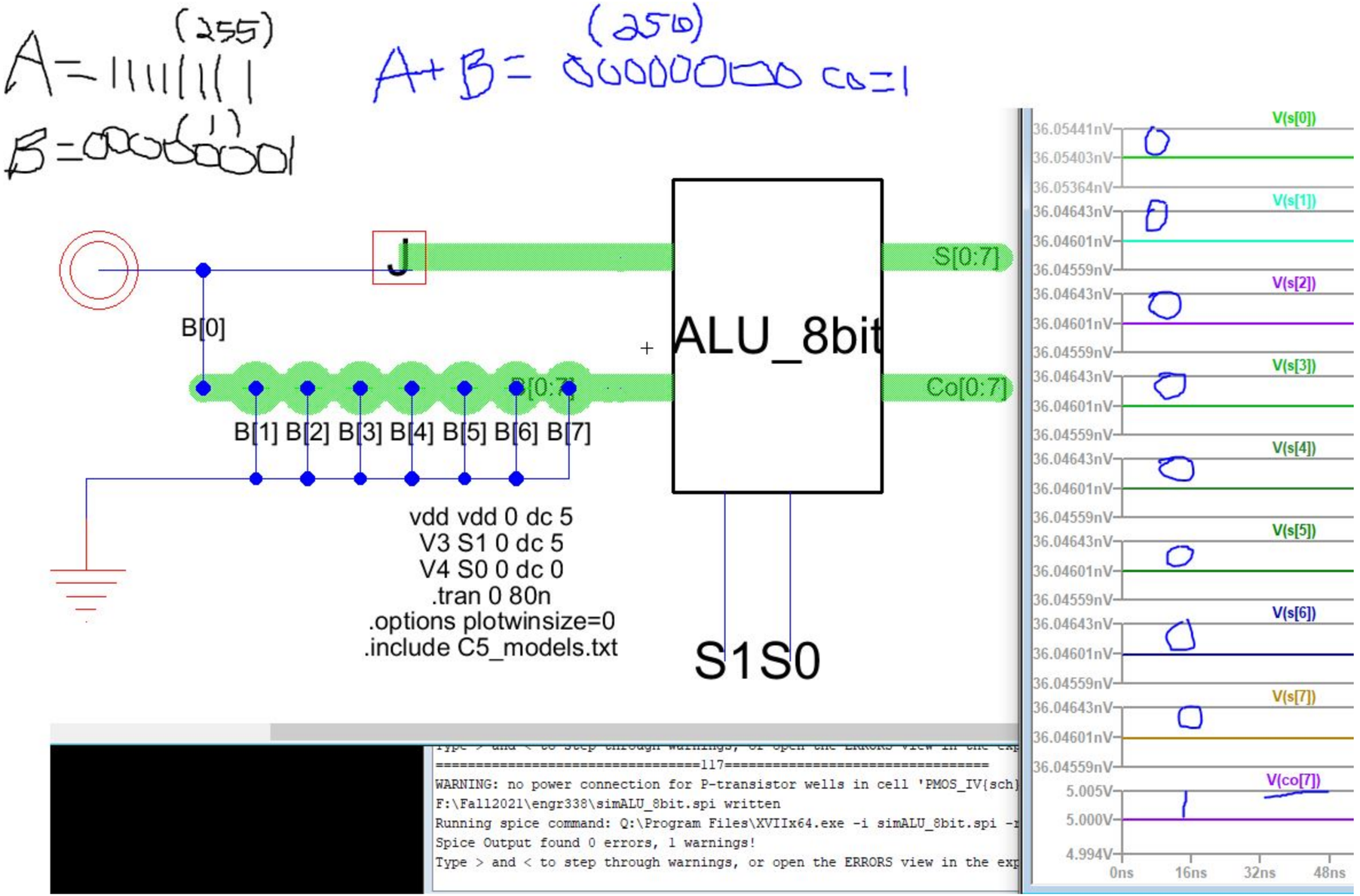
Electric Messages

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 19 networks
Checking cell 'Inverter_Short_8bit_20_10{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.047 secs)
================================497================================
Checking Wells and Substrates in 'ENGR338_Tucson:Inverter_Short_8bit_20_10{lay}'
   Geometry collection found 96 well pieces, took 0.0 secs
   Geometry analysis used 6 threads and took 0.016 secs
NetValues propagation took 0.0 secs
Checking short circuits in 16 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.016 secs)
================================498================================
Hierarchical NCC every cell in the design: cell 'Inverter_Short_8bit_20_10{sch}'
Comparing: ENGR338_Tucson:Inverter_Short_20_10{sch} with: ENGR338_Tucson:Inverte
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:Inverter_Short_8bit_20_10{sch} with: ENGR338_Tucson:In
  exports match, topologies match, sizes not checked in 0.0 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.006 seconds.
```


A[0:7]
B[0:7]
S0 Cin
S1 S1
AND
OR_8bit
MUX_8bit_2_1
Cin
20/10
MUX_8bit_2_1
20/10
MUX_8bit_2_1
FA_HighSpeed_8bit
Cin,Co[0:6]
Cin
Cin
20/10
S1
20/10
S[0:7]
Co[0:7]
A[0:7]
S[0:7]
ALU_8bit
B[0:7]
Co[0:7]
S1 S0
Electric Messages
Checking schematic cell 'ALU_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.009 secs)


vdd vdd 0 dc 5
V3 S1 0 dc 0
V4 S0 0 dc 0
.tran 0 80n
.options plotwinsize=0
.include C5_models.txt
A[0:7]
B[0:7]
ALU_8bit
S[0:7]
Co[0:7]
S1S0
Electric Messages
No errors found
Checking schematic cell 'Inverter_20_10{sch}'
No errors found
Checking schematic cell 'MUX_2_1{sch}'
No errors found
Checking schematic cell 'MUX_8bit_2_1{sch}'
No errors found
Checking schematic cell 'OR{sch}'
No errors found
Checking schematic cell 'OR_8bit{sch}'
No errors found
Checking schematic cell 'ALU_8bit{sch}'
No errors found
Checking schematic cell 'simALU_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.004 secs)
simALU_8bit.spi
V(s[0])
V(s[1])
V(s[2])
V(s[3])
V(s[4])
V(s[5])
V(s[6])
V(s[7])
V(co[7])
84.1286nV
84.1276nV
84.1266nV
6.00783nV
6.00775nV
6.00768nV

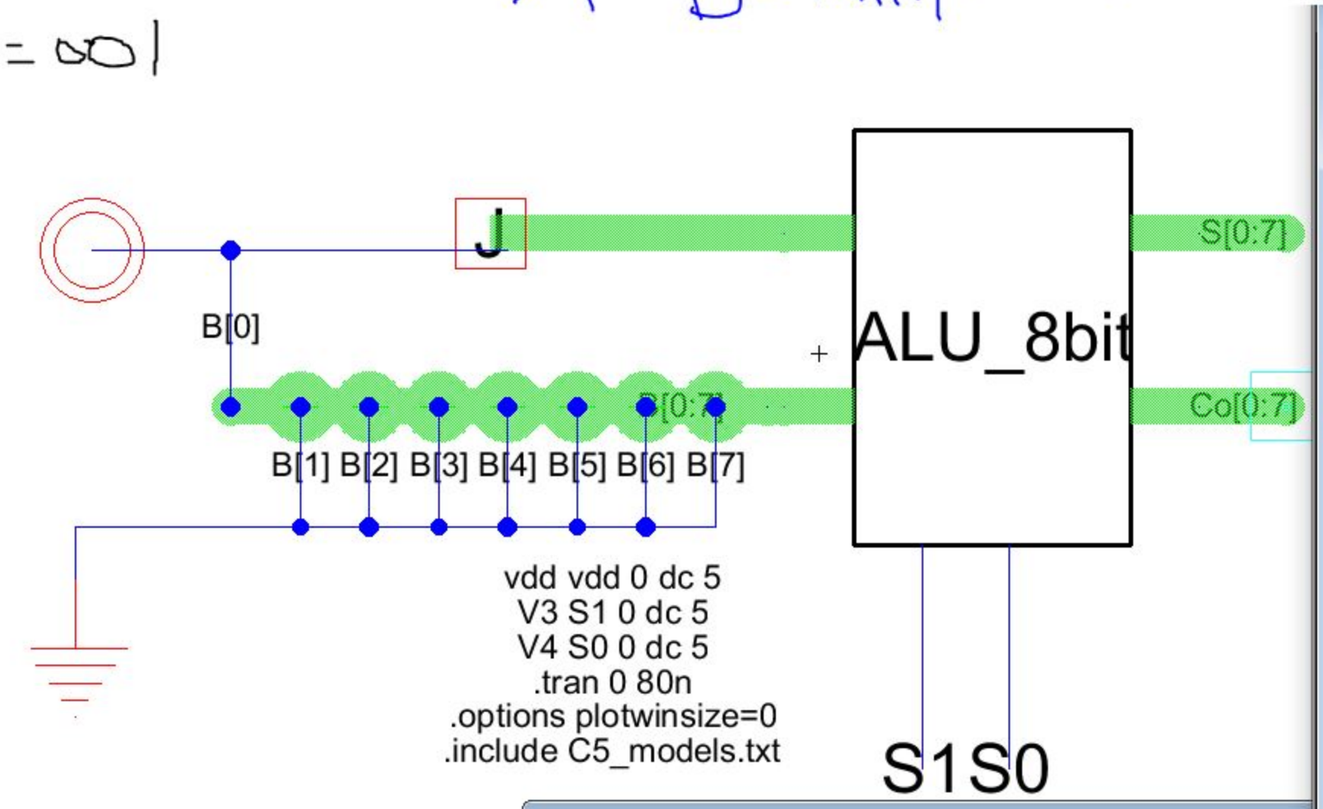

vdd vdd 0 dc 5
V3 S1 0 dc 0
V4 S0 0 dc 5
.tran 0 80n
.options plotwinsize=0
.include C5_models.txt
A[0:7]
B[0:7]
ALU_8bit
S[0:7]
Co[0:7]
S1S0
Electric Messages
No errors found
Checking schematic cell 'MUX_8bit_2_1{sch}'
No errors found
Checking schematic cell 'OR{sch}'
No errors found
Checking schematic cell 'OR_8bit{sch}'
No errors found
Checking schematic cell 'ALU_8bit{sch}'
No errors found
Checking schematic cell 'simALU_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.007 secs)
simALU_8bit.spi
V(s[0])
V(s[1])
V(s[2])
V(s[3])
V(s[4])
V(s[5])
V(s[6])
V(s[7])
V(co[7])
5.005V
5.000V
4.994V
0ns
16ns
32ns
48ns
64ns

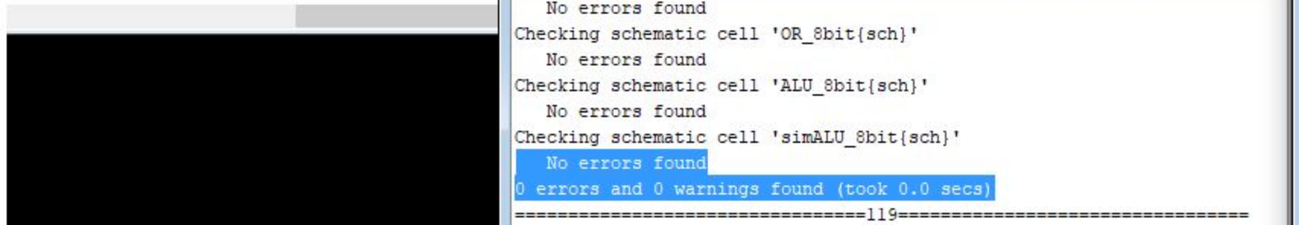

A=11111111 (255)
B=00000001 (1)
A+B= 100000000 (256) Co=1
J
S[0:7]
B[0]
B[1] B[2] B[3] B[4] B[5] B[6] B[7]
ALU_8bit
Co[0:7]
vdd vdd 0 dc 5
V3 S1 0 dc 5
V4 S0 0 dc 0
.tran 0 80n
.options plotwinsize=0
.include C5_models.txt
S1S0
V(s[0])
V(s[1])
V(s[2])
V(s[3])
V(s[4])
V(s[5])
V(s[6])
V(s[7])
V(co[7])
36.05441nV
36.05403nV
36.05364nV
36.04643nV
36.04601nV
36.04559nV
5.005V
5.000V
4.994V
0ns
16ns
32ns
48ns
==========117==========
WARNING: no power connection for P-transistor wells in cell 'PMOS_IV{sch}
F:\Fall2021\engr338\simALU_8bit.spi written
Running spice command: Q:\Program Files\XVIIx64.exe -i simALU_8bit.spi -r
Spice Output found 0 errors, 1 warnings!
Type > and < to step through warnings, or open the ERRORS view in the exp

A=255

B=001

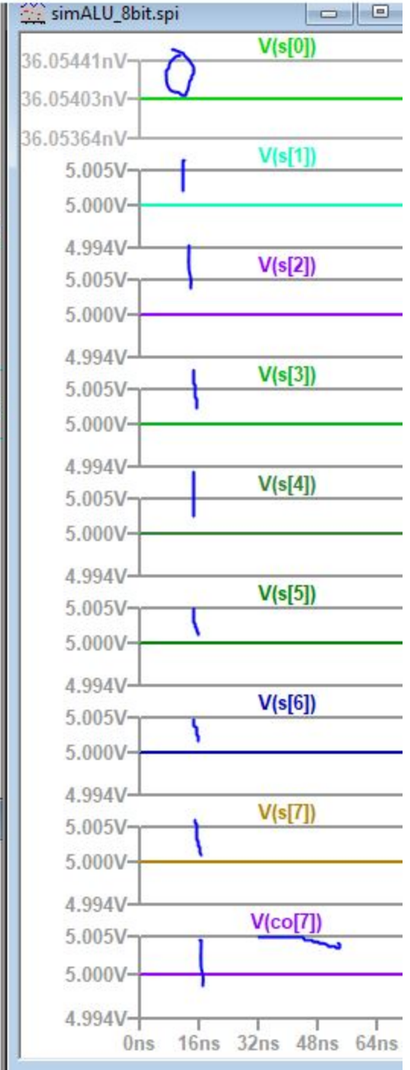
A-B=11111110 (254) Co=1

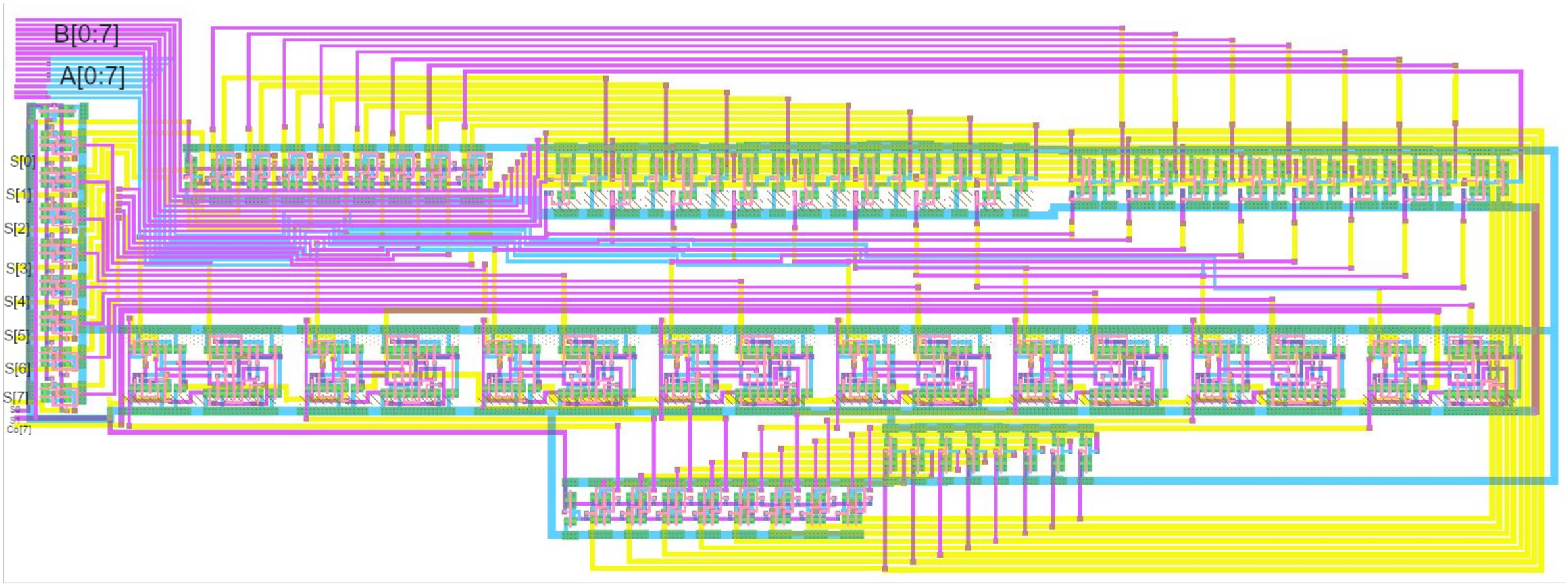


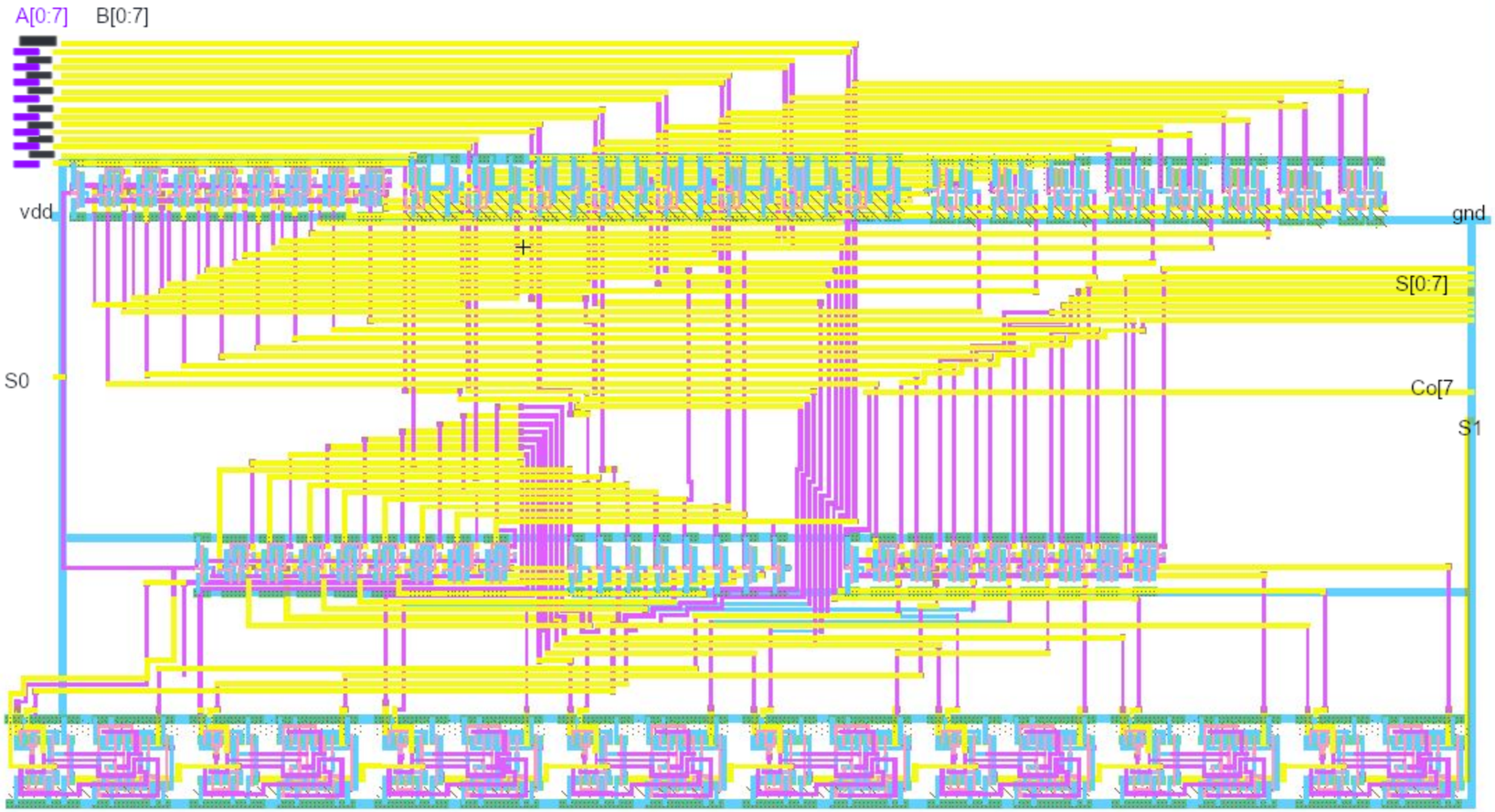


Electric Messages

```
   No errors found
Checking schematic cell 'OR_8bit{sch}'
   No errors found
Checking schematic cell 'ALU_8bit{sch}'
   No errors found
Checking schematic cell 'simALU_8bit{sch}'
   No errors found
0 errors and 0 warnings found (took 0.0 secs)
==================================119==================================
```




B[0:7]
A[0:7]
S[0]
S[1]
S[2]
S[3]
S[4]
S[5]
S[6]
S[7]
Co[7]




```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 88 networks
0 errors and 0 warnings found (took 0.016 secs)
[redacted]==========13254==========
Checking Wells and Substrates in 'ENGR338_Tucson:ALU_8bit{lay}' ...
   Geometry collection found 2700 well pieces, took 0.016 secs
   Geometry analysis used 6 threads and took 0.0 secs
NetValues propagation took 0.0 secs
Checking short circuits in 166 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.016 secs)
[redacted]==========13255==========
Hierarchical NCC every cell in the design: cell 'ALU_8bit{sch}'  cell 'ALU_8bit{lay}'
Comparing: ENGR338_Tucson:AND{sch} with: ENGR338_Tucson:AND{lay}
  exports match, topologies match, sizes not checked in 0.007 seconds.
Comparing: ENGR338_Tucson:AND_8bit{sch} with: ENGR338_Tucson:AND_8bit{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:FA_HighSpeed_1bit{sch} with: ENGR338_Tucson:FA_HighSpeed_1bi
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:FA_HighSpeed_8bit{sch} with: ENGR338_Tucson:FA_HighSpeed_8bi
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:Inverter_Short_20_10{sch} with: ENGR338_Tucson:Inverter_Shor
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:Inverter_Short_8bit_20_10{sch} with: ENGR338_Tucson:Inverter
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:MUX_2_1{sch} with: ENGR338_Tucson:MUX_2_1{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:MUX_8bit_2_1{sch} with: ENGR338_Tucson:MUX_8bit_2_1{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:OR{sch} with: ENGR338_Tucson:OR{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:OR_8bit{sch} with: ENGR338_Tucson:OR_8bit{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:ALU_8bit{sch} with: ENGR338_Tucson:ALU_8bit{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.007 seconds.
```