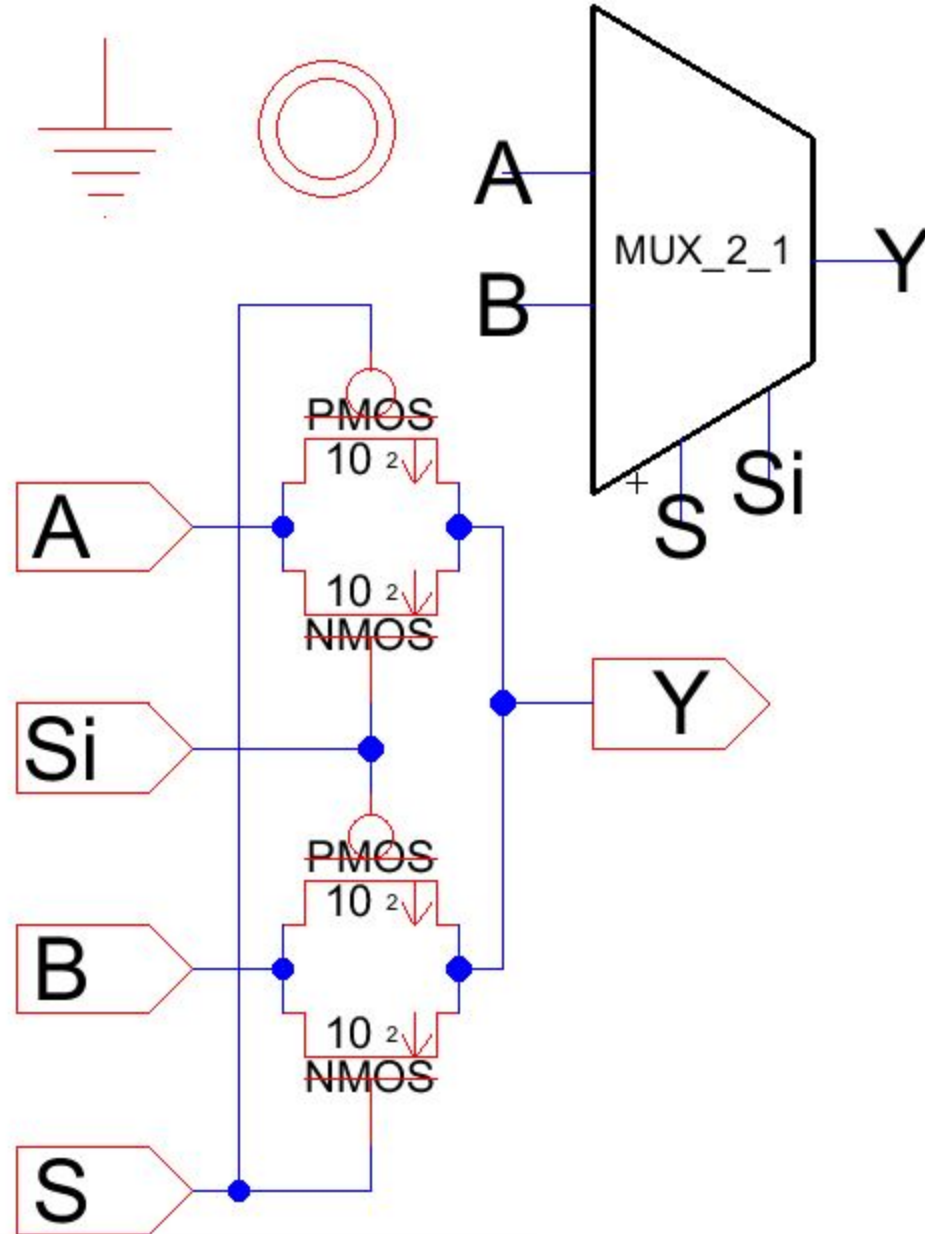
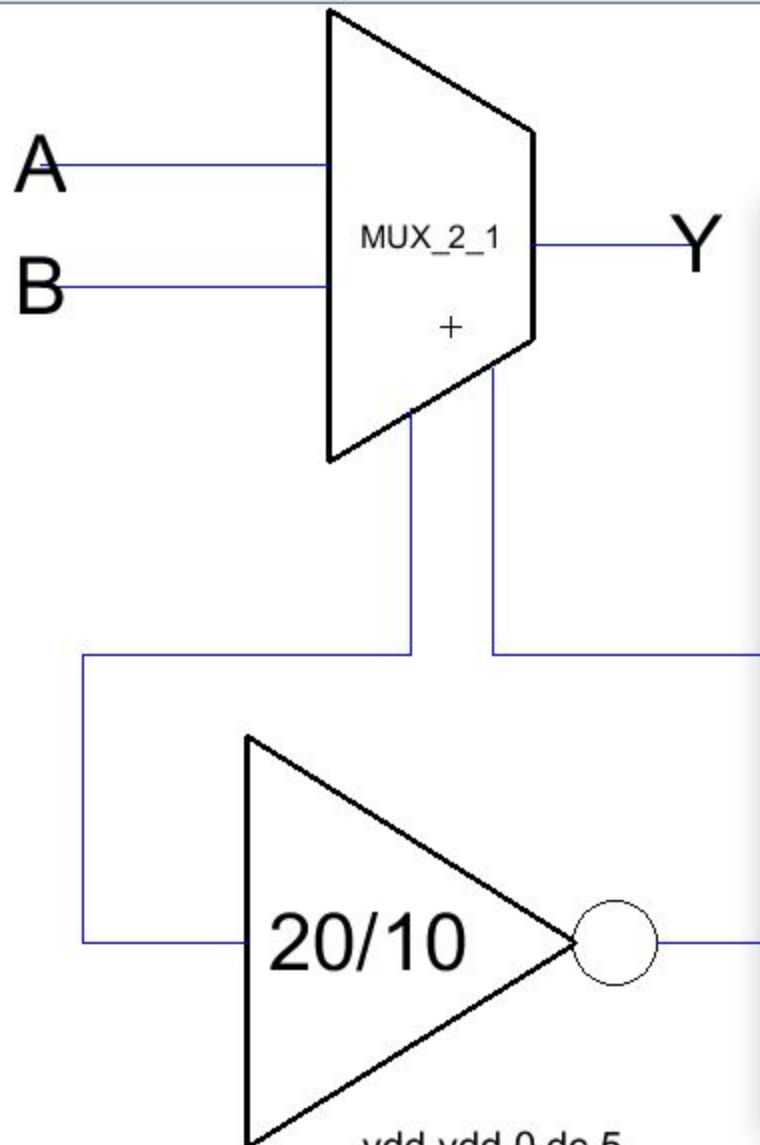




Checking schematic cell 'MUX_2_1{sch}'

No errors found

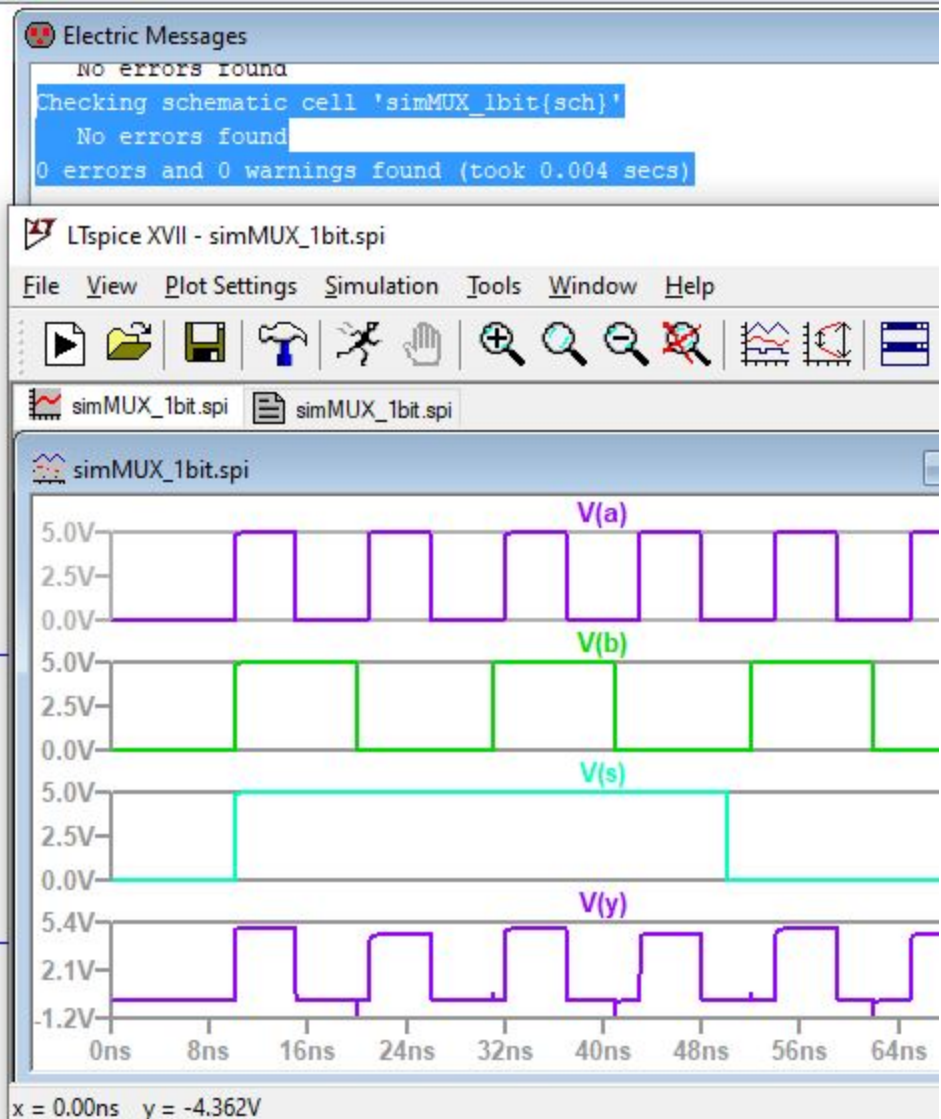
0 errors and 0 warnings found (took 0.002 secs)

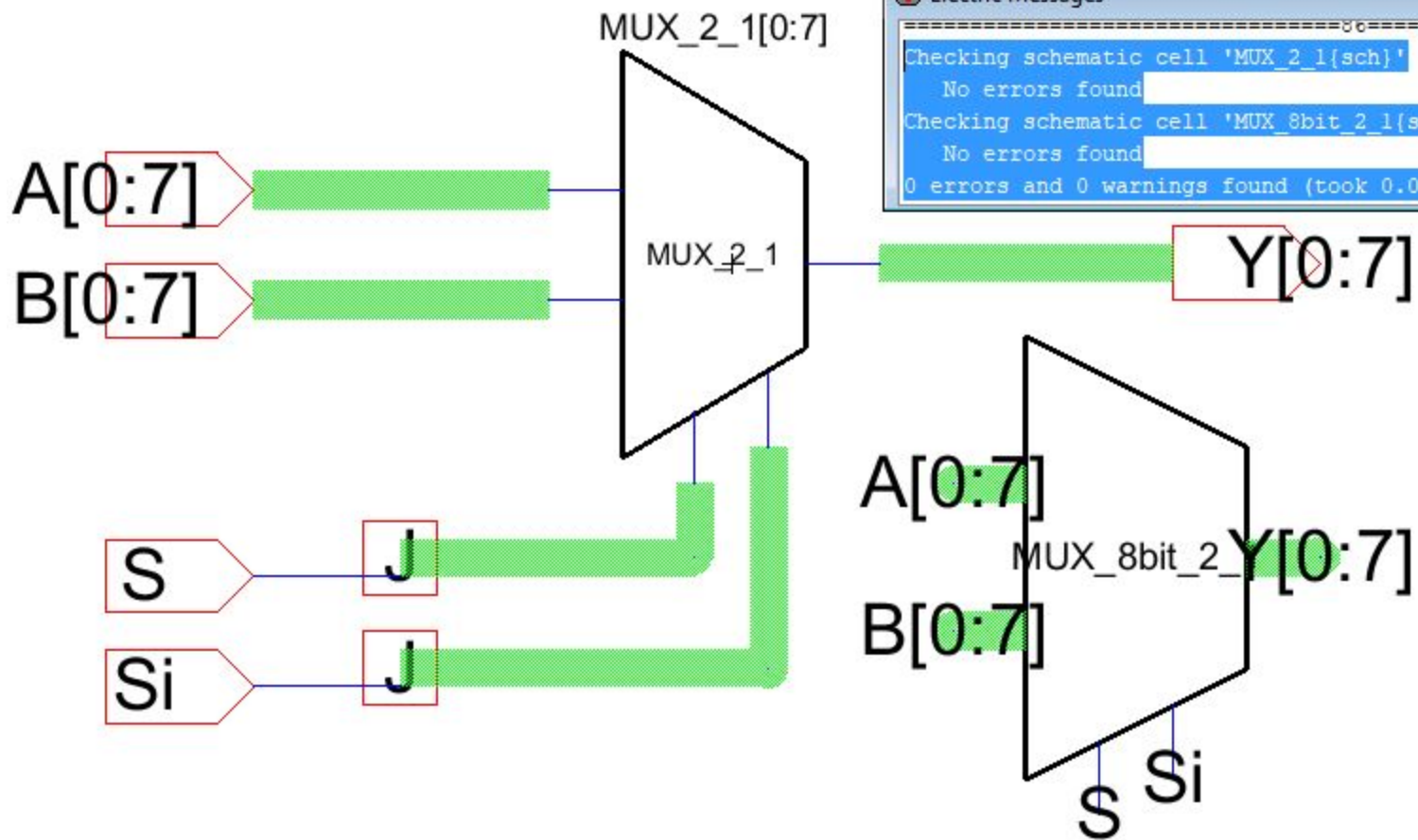


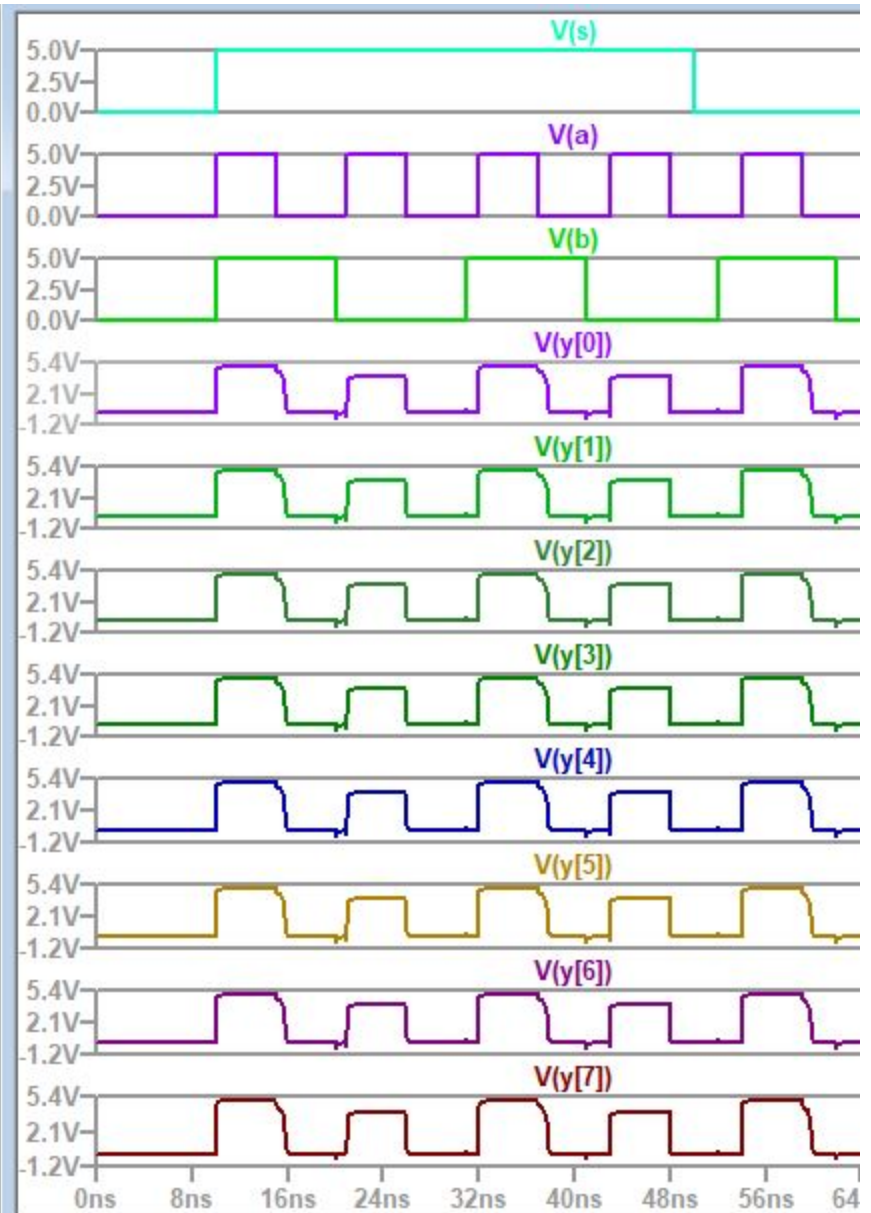
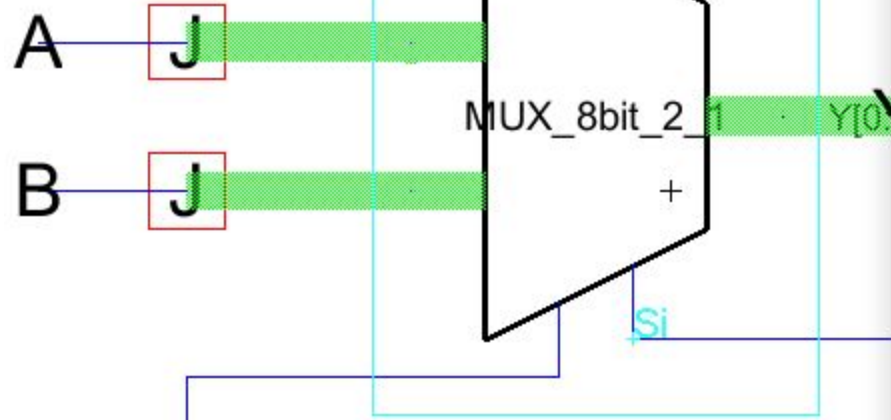
```

vdd vdd 0 dc 5
V1 A 0 PULSE(0 5 10n 1p 1p 5n 11n)
V2 B 0 PULSE(0 5 10n 1p 1p 10n 21n)
V3 S 0 PULSE(0 5 10n 1p 1p 40n 81n)
.tran 0 80n
.options plotwinsize=0
.include C5_models.txt

```







```

vdd vdd 0 dc 5
V1 A 0 PULSE(0 5 10n 1p 1p 5n 11n)
V2 B 0 PULSE(0 5 10n 1p 1p 10n 21n)
V3 S 0 PULSE(0 5 10n 1p 1p 40n 81n)
.tran 0 80n
.options plotwinsize=0
.include C5_models.txt

```

Electric Messages

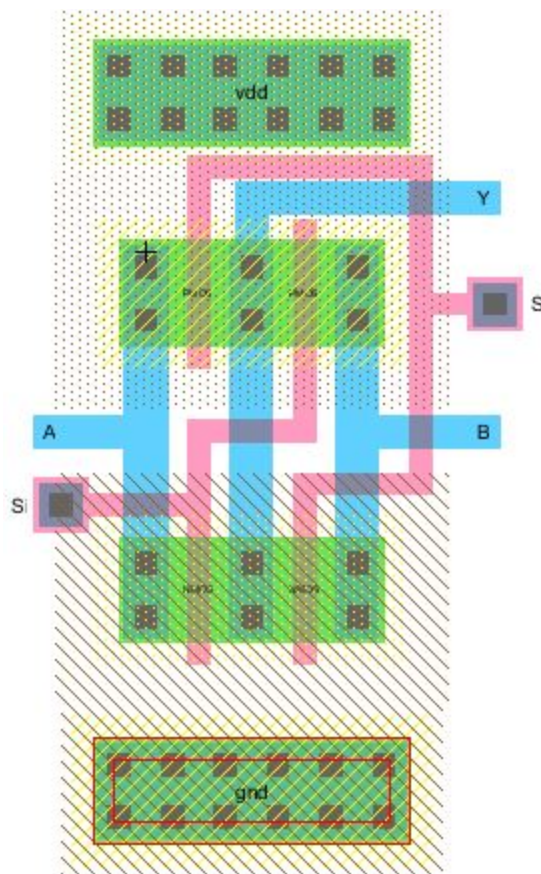
Checking schematic

No errors found

Checking schematic cell 'simMUX_8bit(sch)'

No errors found

0 errors and 0 warnings found (took 0.003 secs)



Running DRC with area bit on, extension bit on, Mosis bit

Checking again hierarchy (0.0 secs)

Found 12 networks

Checking cell 'MUX_2_1{lay}'

No errors/warnings found

0 errors and 0 warnings found (took 0.028 secs)

=====280=====

Checking Wells and Substrates in 'ENGR338_Tucson:MUX_2_1{lay}' ...

Geometry collection found 20 well pieces, took 0.0 secs

Geometry analysis used 6 threads and took 0.002 secs

NetValues propagation took 0.0 secs

Checking short circuits in 2 well contacts

Additional analysis took 0.0 secs

No Well errors found (took 0.002 secs)

=====281=====

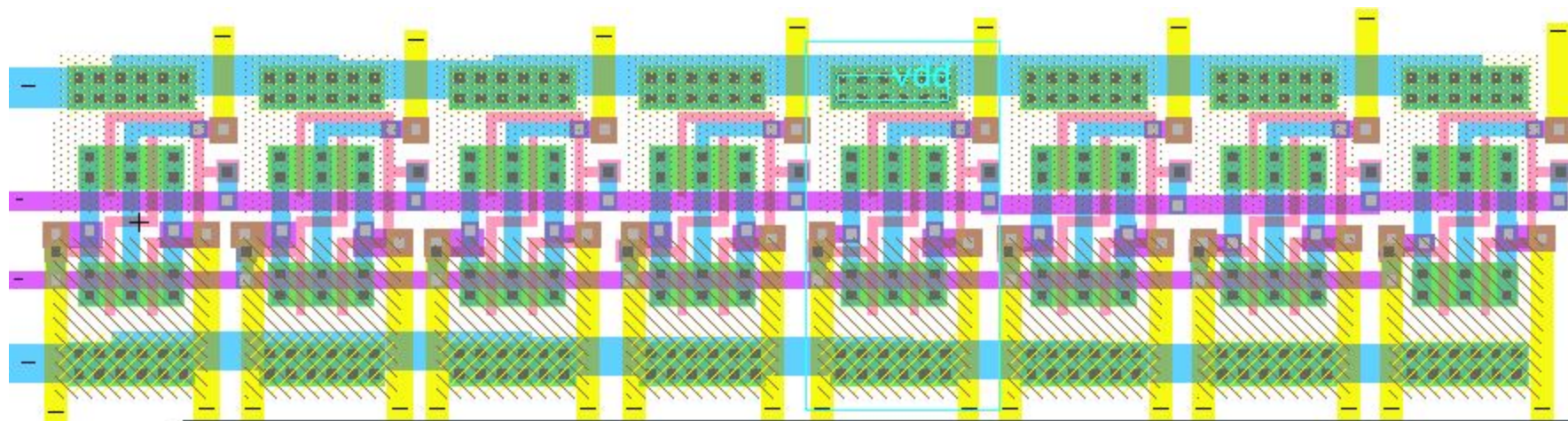
Hierarchical NCC every cell in the design: cell 'MUX_2_1{sch}' cell 'MUX_2_1{lay}

Comparing: ENGR338_Tucson:MUX_2_1{sch} with: ENGR338_Tucson:MUX_2_1{lay}

exports match, topologies match, sizes not checked in 0.033 seconds.

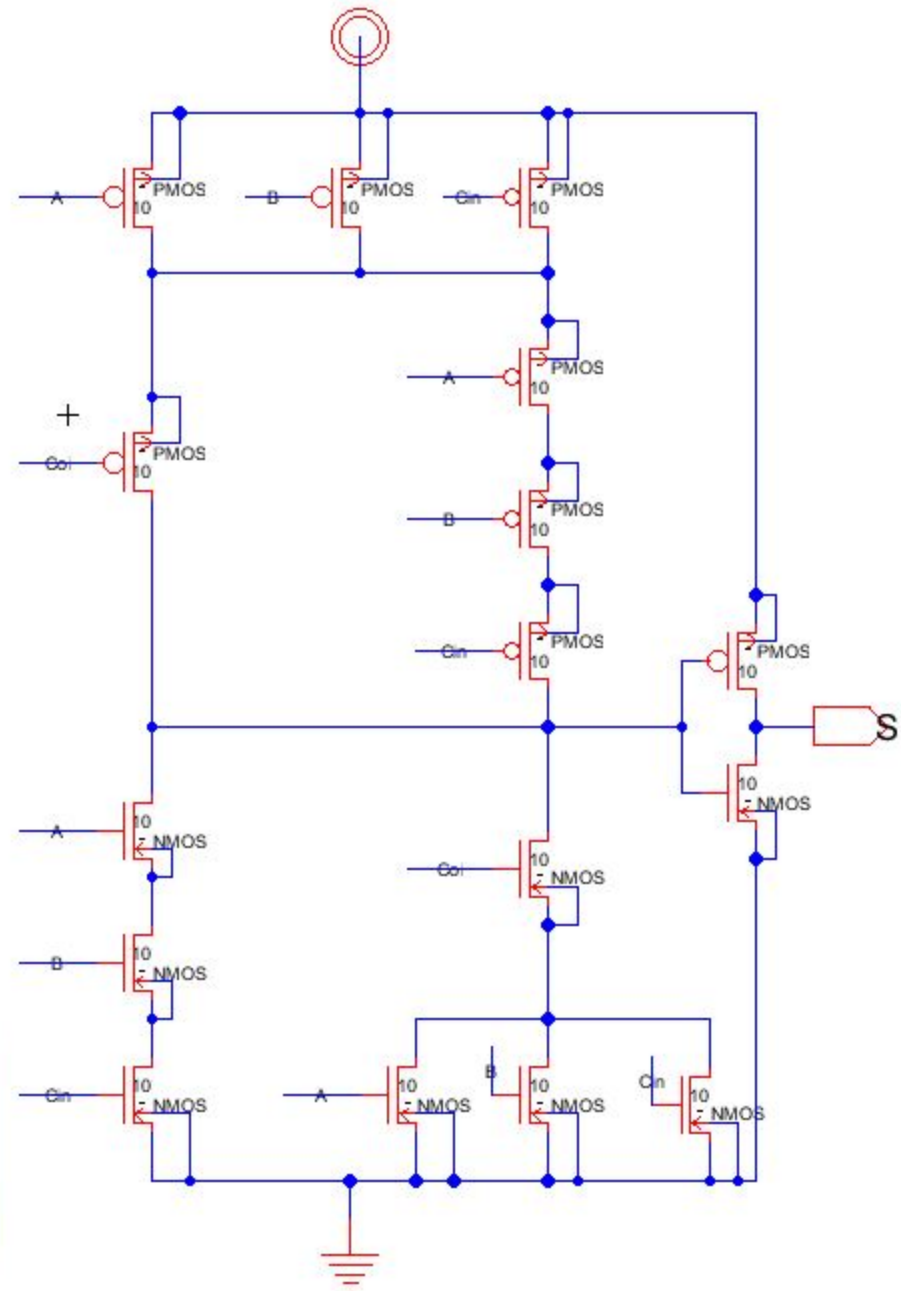
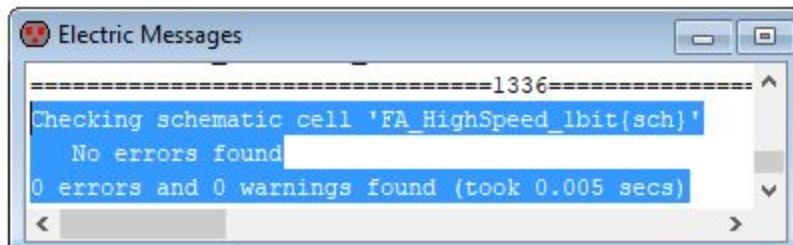
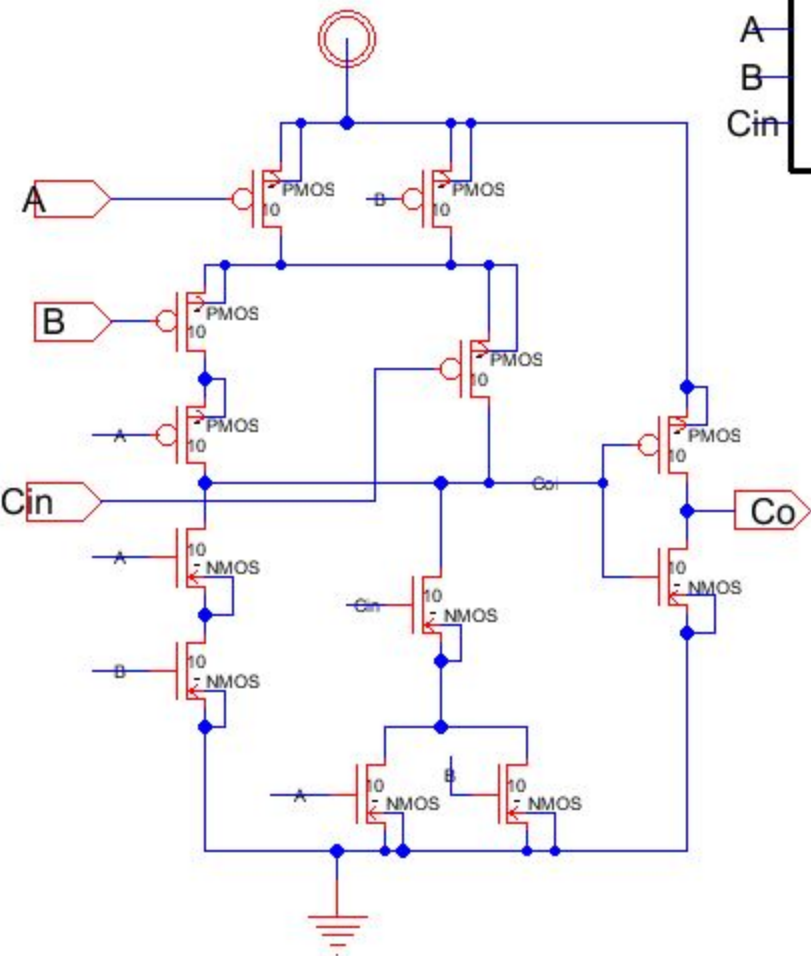
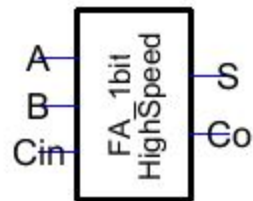
Summary for all cells: exports match, topologies match, sizes not checked

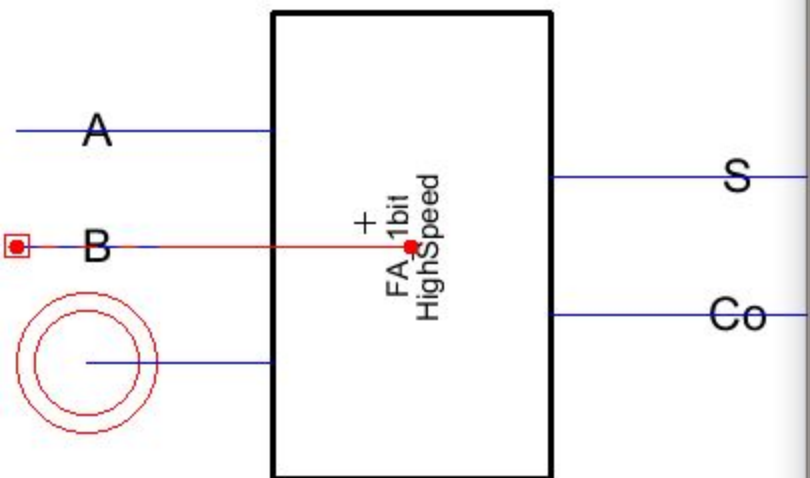
NCC command completed in: 0.042 seconds.



Electric Messages

```
=====910=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 29 networks
0 errors and 0 warnings found (took 0.001 secs)
=====911=====
Checking Wells and Substrates in 'ENGR338_Tucson:MUX_8bit_2_1{lay}' ...
  Geometry collection found 160 well pieces, took 0.002 secs
  Geometry analysis used 6 threads and took 0.002 secs
NetValues propagation took 0.0 secs
Checking short circuits in 16 well contacts
  Additional analysis took 0.0 secs
No Well errors found (took 0.004 secs)
=====912=====
Hierarchical NCC every cell in the design: cell 'MUX_8bit_2_1{sch}' cell 'MUX_8bit_2_1{lay}'
Comparing: ENGR338_Tucson:MUX_2_1{sch} with: ENGR338_Tucson:MUX_2_1{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338_Tucson:MUX_8bit_2_1{sch} with: ENGR338_Tucson:MUX_8bit_2_1{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.004 seconds.
```

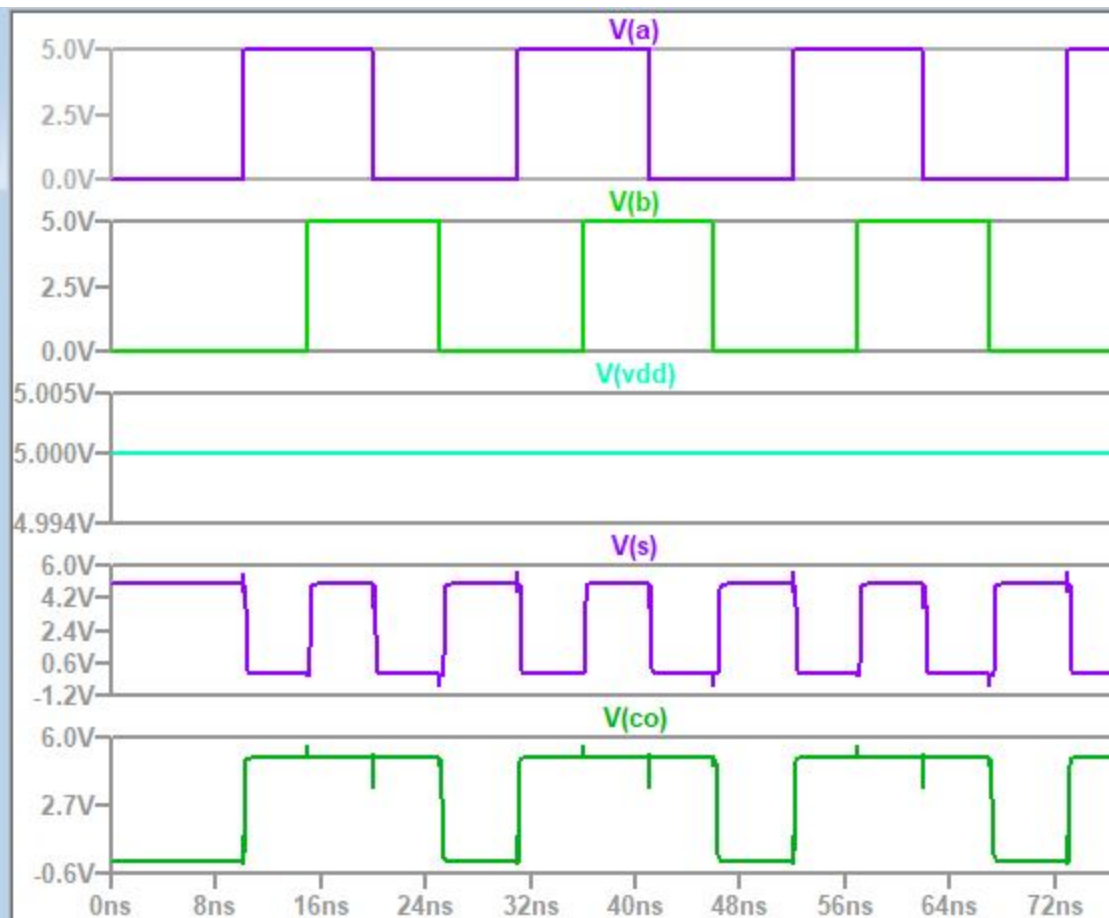




```

vdd vdd 0 dc 5
V1 A 0 PULSE(0 5 10n 1p 1p 10n 21n)
V2 B 0 PULSE(0 5 15n 1p 1p 10n 21n)
.tran 0 80n
.options plotwinsize=0
.include C5_models.txt

```





```

-----
0 errors and 0 warnings found (took 0.009 secs)
=====169=====
Checking schematic cell 'FA_HighSpeed_1bit{sch}'
  No errors found
Checking schematic cell 'FA_HighSpeed_8bit{sch}'
  No errors found
0 errors and 0 warnings found (took 0.003 secs)

```

