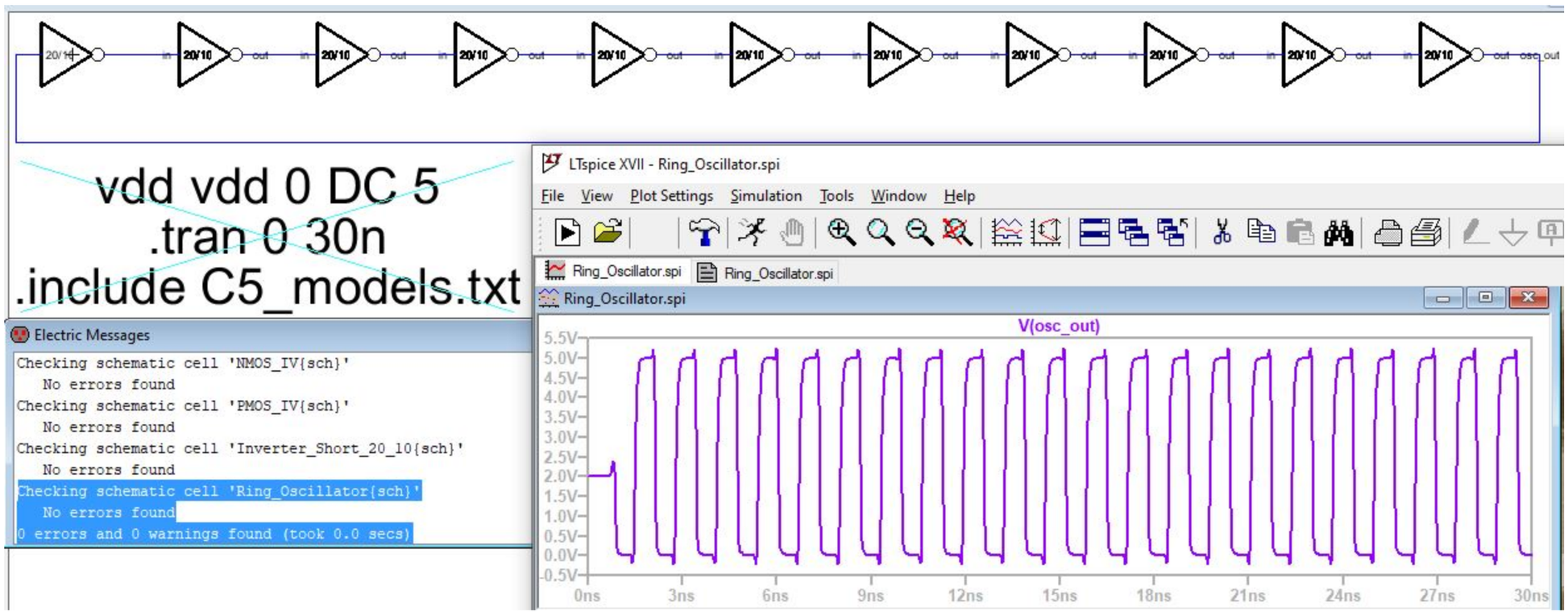
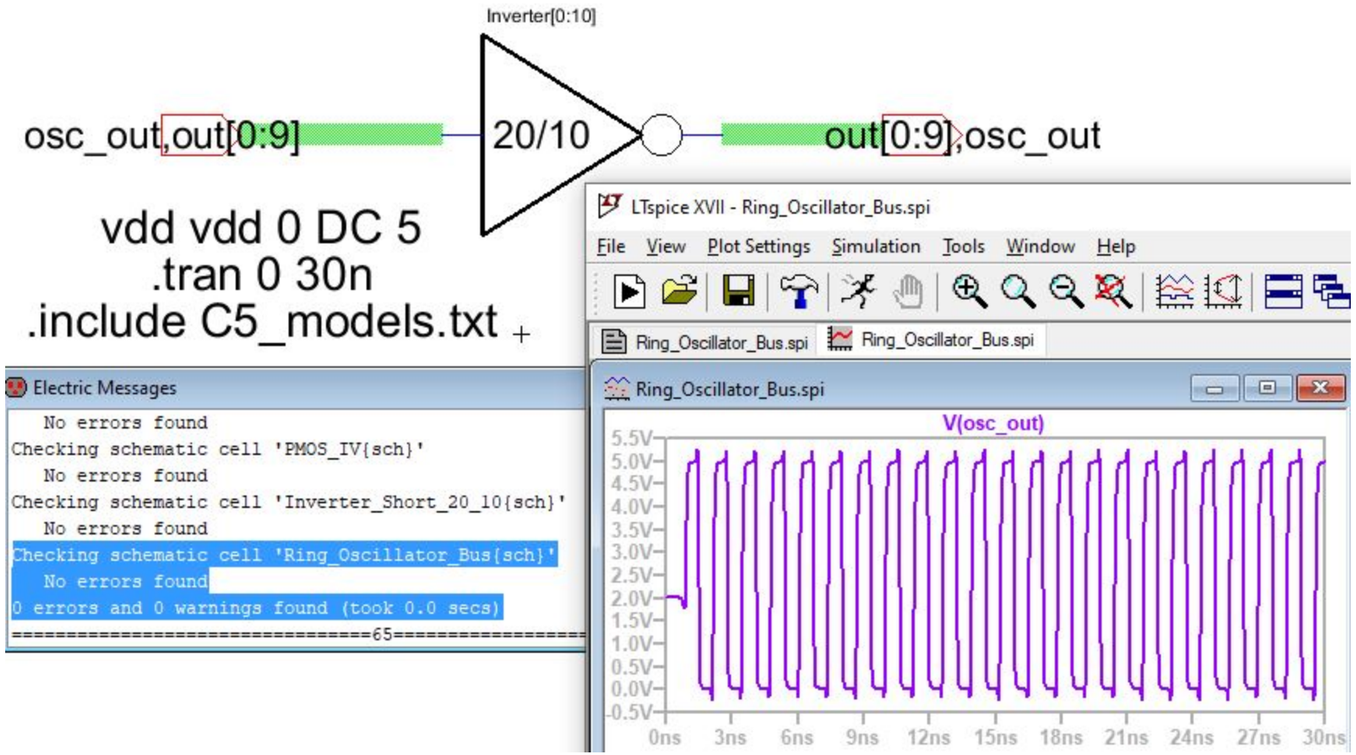
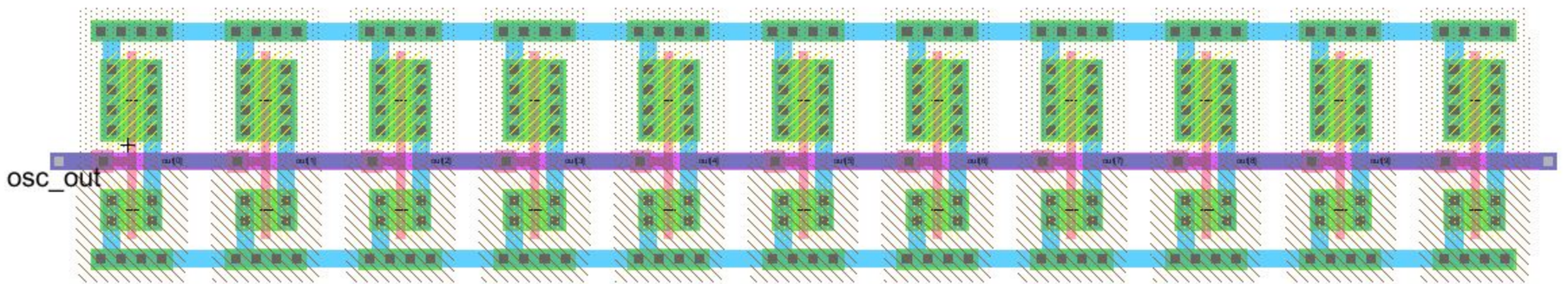
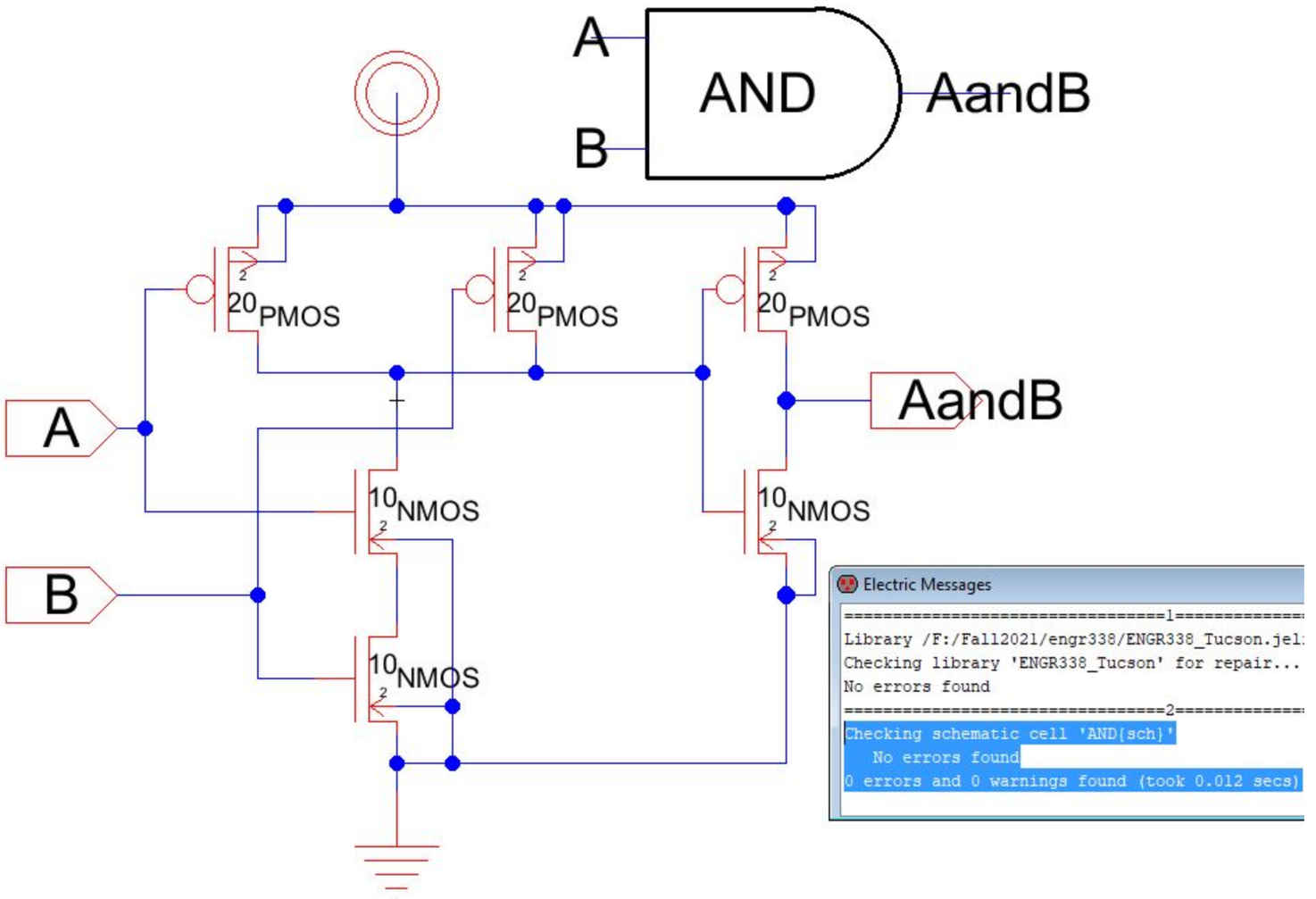
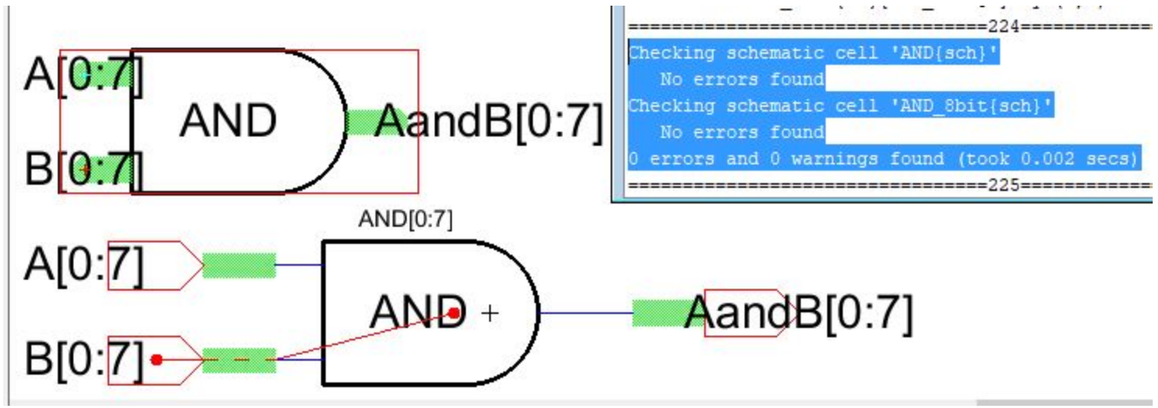

20/10
in
out
osc_out
vdd vdd 0 DC 5
.tran 0 30n
.include C5_models.txt
Electric Messages
Checking schematic cell 'NMOS_IV{sch}'
No errors found
Checking schematic cell 'PMOS_IV{sch}'
No errors found
Checking schematic cell 'Inverter_Short_20_10{sch}'
No errors found
Checking schematic cell 'Ring_Oscillator{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)
LTspice XVII - Ring_Oscillator.spi
File View Plot Settings Simulation Tools Window Help
Ring_Oscillator.spi
Ring_Oscillator.spi
Ring_Oscillator.spi
V(osc_out)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0ns
3ns
6ns
9ns
12ns
15ns
18ns
21ns
24ns
27ns
30ns

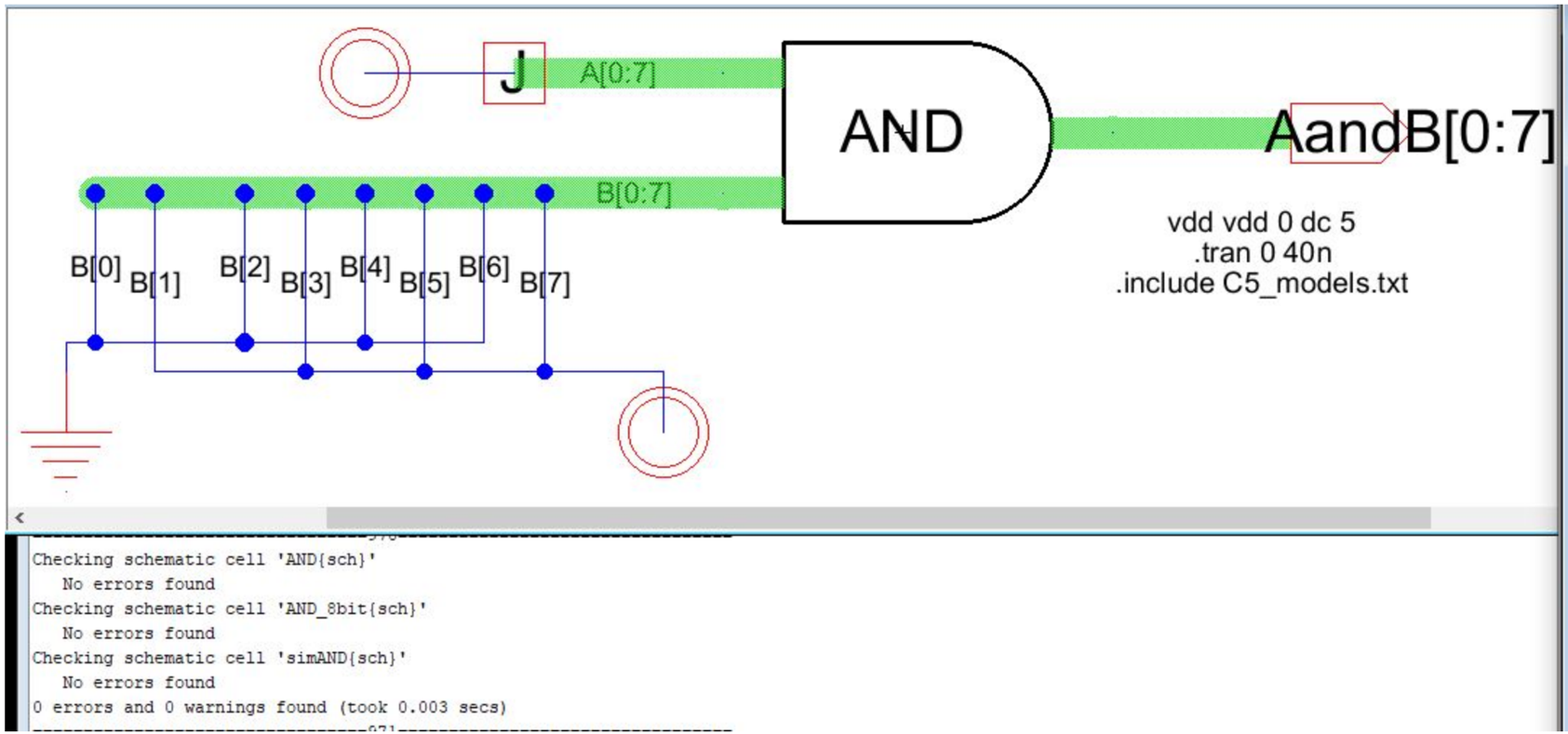

Inverter[0:10]
osc_out,out[0:9]
20/10
out[0:9],osc_out
vdd vdd 0 DC 5
.tran 0 30n
.include C5_models.txt +
Electric Messages
No errors found
Checking schematic cell 'PMOS_IV{sch}'
No errors found
Checking schematic cell 'Inverter_Short_20_10{sch}'
No errors found
Checking schematic cell 'Ring_Oscillator_Bus{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)
LTspice XVII - Ring_Oscillator_Bus.spi
File View Plot Settings Simulation Tools Window Help
Ring_Oscillator_Bus.spi
Ring_Oscillator_Bus.spi
Ring_Oscillator_Bus.spi
V(osc_out)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0ns
3ns
6ns
9ns
12ns
15ns
18ns
21ns
24ns
27ns
30ns



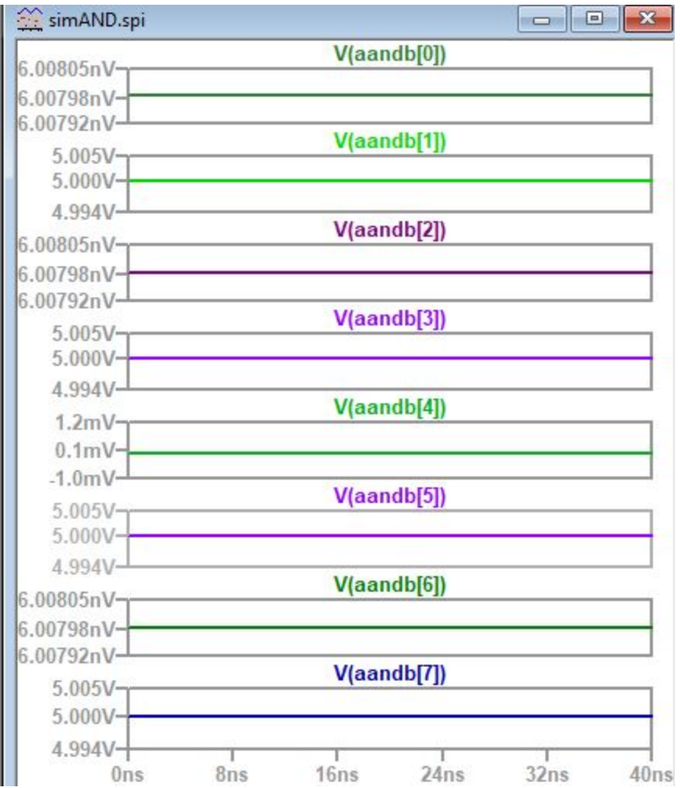

```
Checking cell 'Ring_Oscillator_Bus{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.029 secs)
```

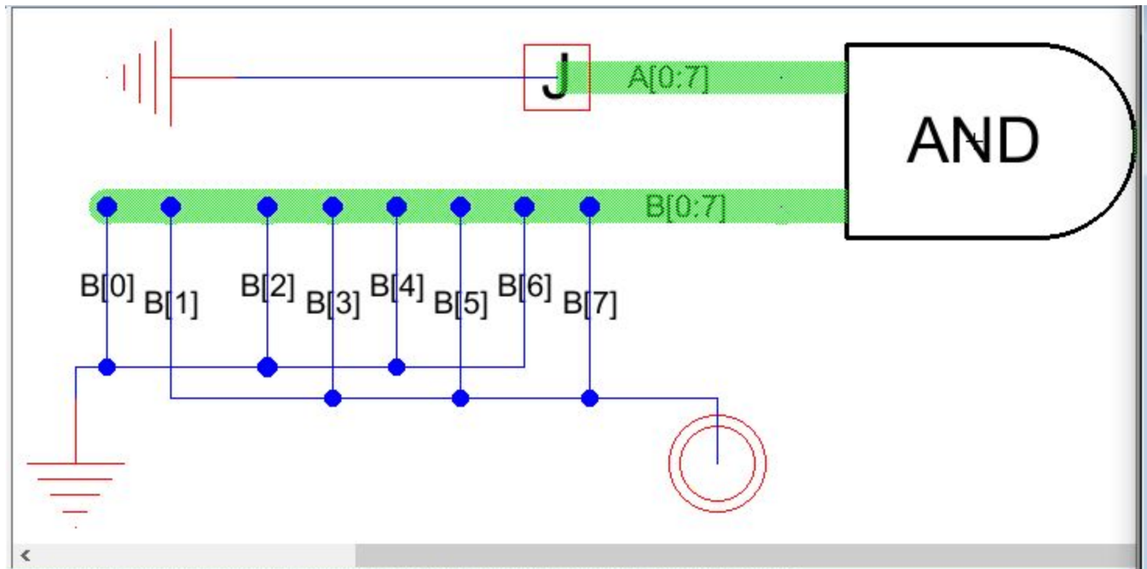

A
B
AND
AandB
20PMOS
20PMOS
20PMOS
A
B
AandB
10NMOS
10NMOS
10NMOS
Electric Messages
Library /F:/Fall2021/engr338/ENGR338_Tucson.jel
Checking library 'ENGR338_Tucson' for repair...
No errors found
Checking schematic cell 'AND{sch}'
No errors found
0 errors and 0 warnings found (took 0.012 secs)


A[0:7]
B[0:7]
AND
AandB[0:7]
AND[0:7]
A[0:7]
B[0:7]
AND
AandB[0:7]
==========224==========
Checking schematic cell 'AND{sch}'
No errors found
Checking schematic cell 'AND_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.002 secs)
==========225==========

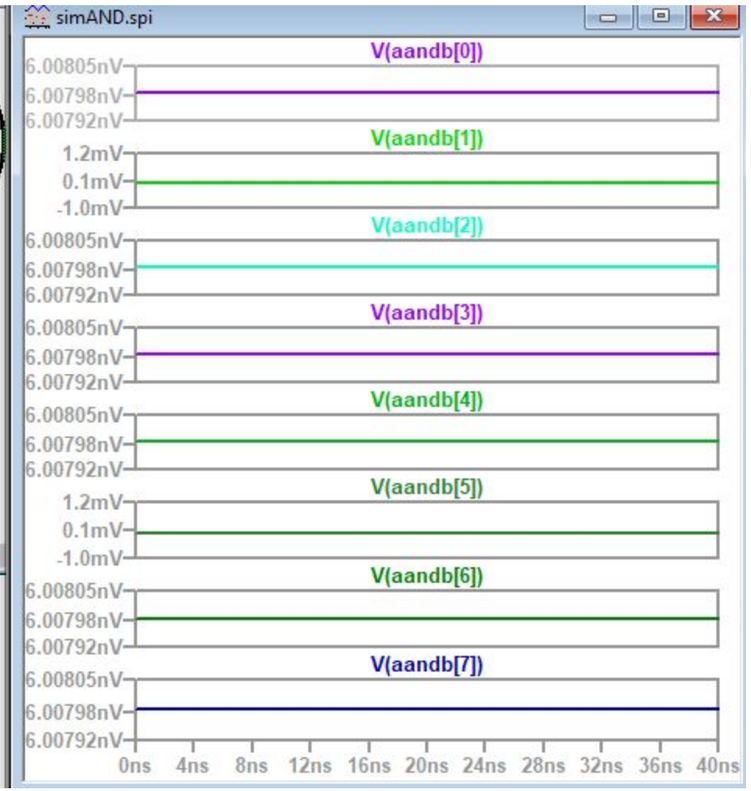


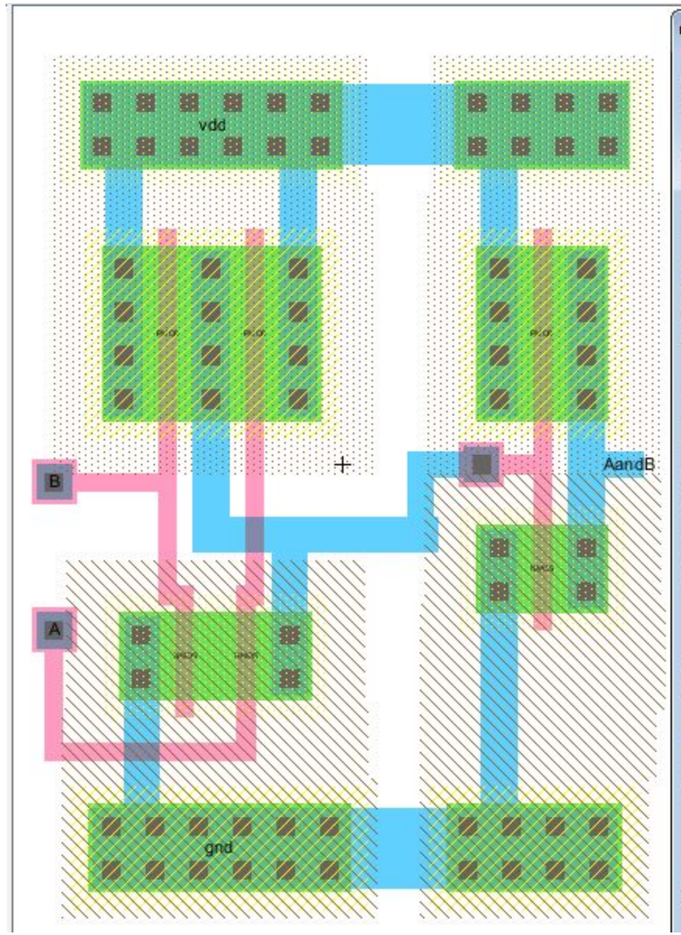

```
Checking schematic cell 'AND{sch}'
   No errors found
Checking schematic cell 'AND_8bit{sch}'
   No errors found
Checking schematic cell 'simAND{sch}'
   No errors found
0 errors and 0 warnings found (took 0.003 secs)
```





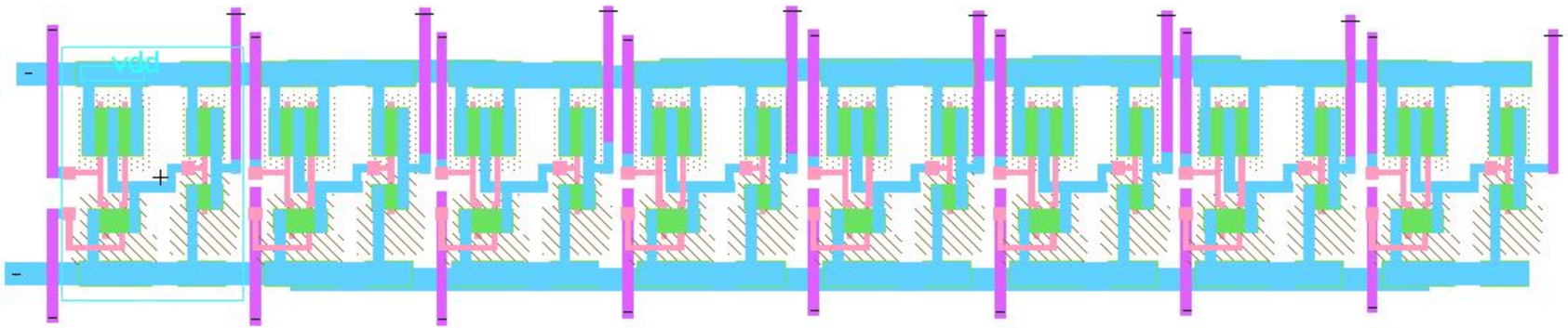

```
Checking schematic cell 'AND{sch}'
   No errors found
Checking schematic cell 'AND_8bit{sch}'
   No errors found
Checking schematic cell 'simAND{sch}'
   No errors found
0 errors and 0 warnings found (took 0.003 secs)
```





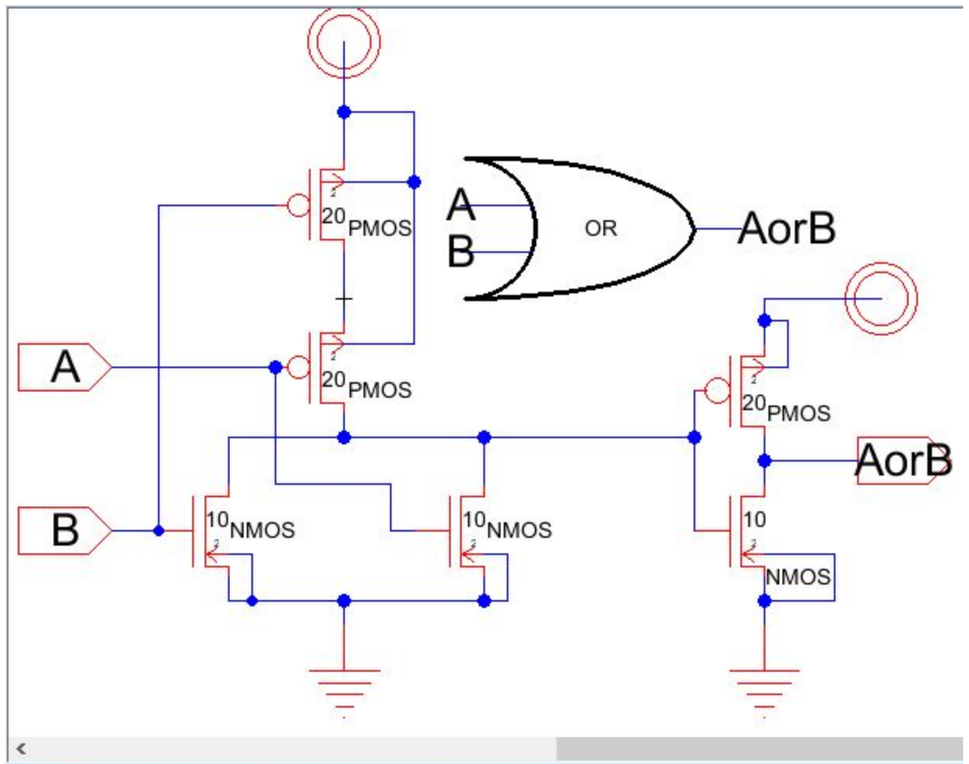
Electric Messages

```
NetValues propagation took 0.0 secs
Checking short circuits in 4 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.004 secs)
================================1122============================
F:\Fall2021\engr338\ENGR338_Tucson.jelib written
================================1123============================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 23 networks
Checking cell 'AND{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.026 secs)
================================1124============================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 23 networks
0 errors and 0 warnings found (took 0.001 secs)
================================1125============================
Checking Wells and Substrates in 'ENGR338_Tucson:AND{lay}' ...
   Geometry collection found 39 well pieces, took 0.001 secs
   Geometry analysis used 6 threads and took 0.003 secs
NetValues propagation took 0.0 secs
Checking short circuits in 4 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.004 secs)
================================1126============================
Hierarchical NCC every cell in the design: cell 'AND{sch}'  cell
Comparing: ENGR338_Tucson:AND{sch} with: ENGR338_Tucson:AND{lay}
  exports match, topologies match, sizes not checked in 0.034 se
Summary for all cells: exports match, topologies match, sizes no
NCC command completed in: 0.042 seconds.
```

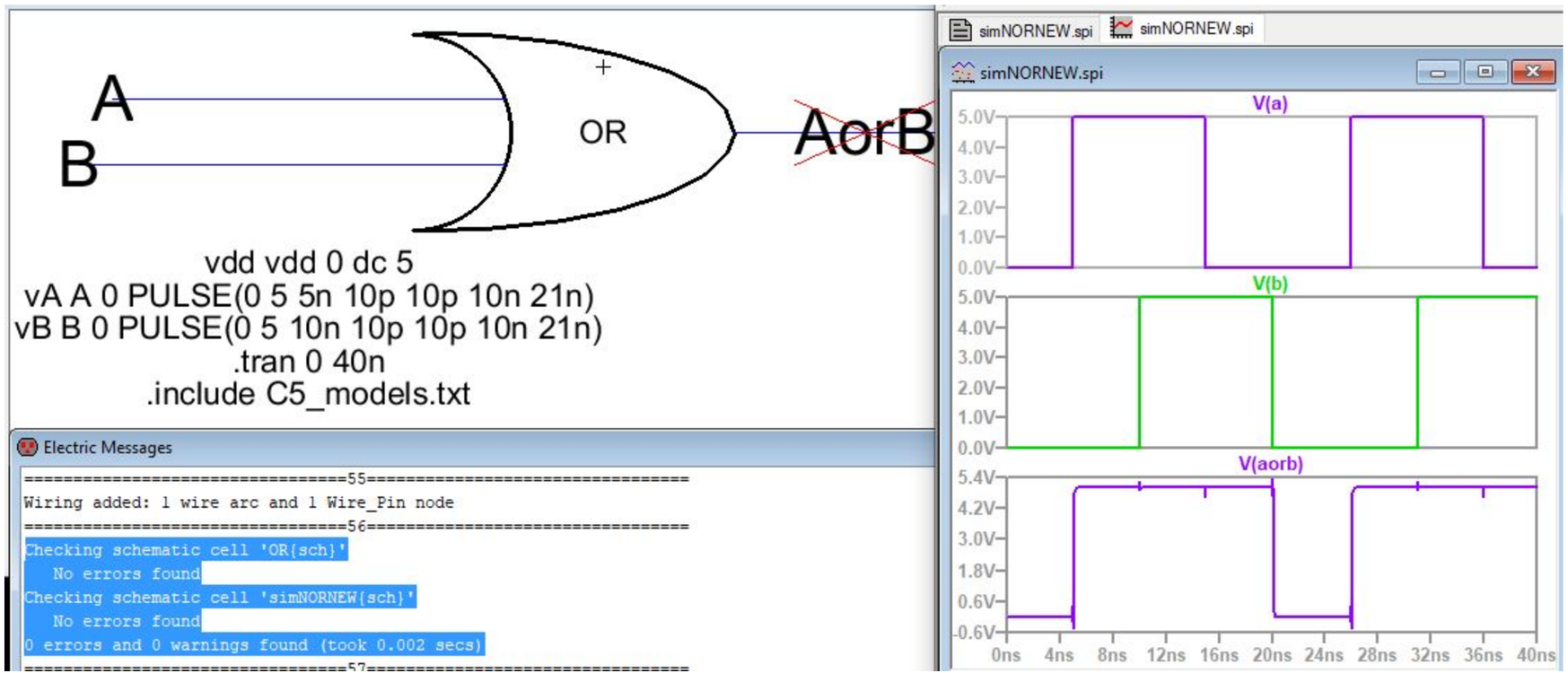


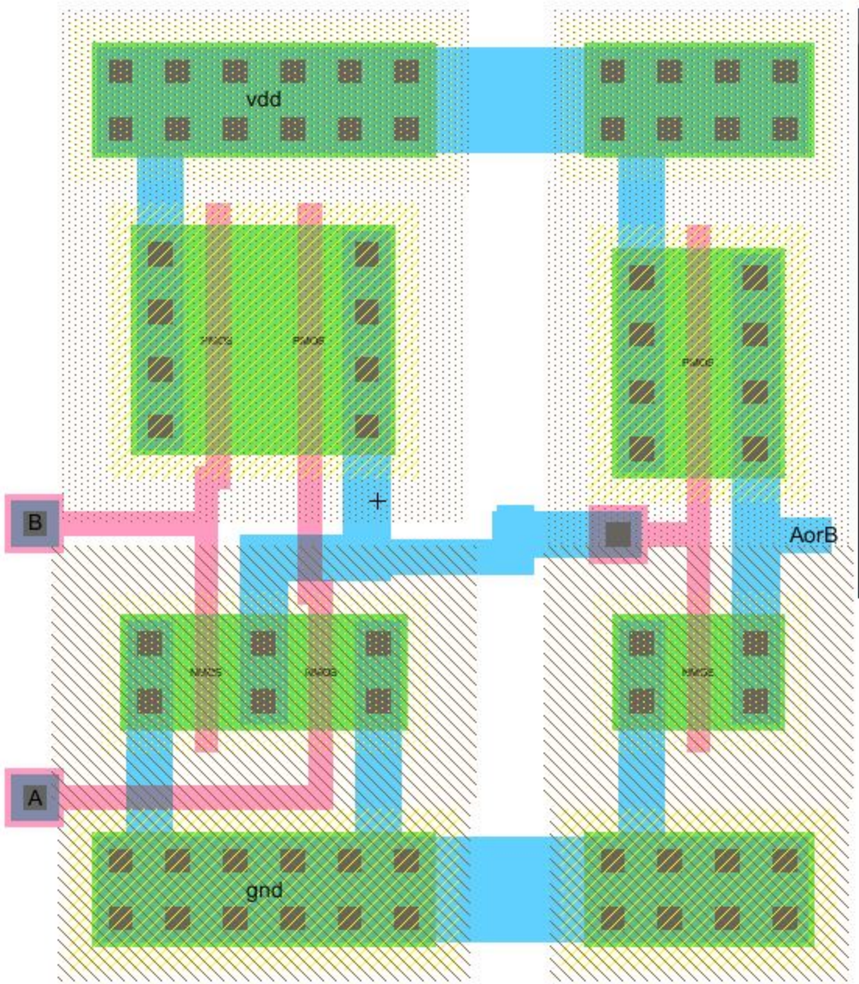
Electric Messages

```
Found 27 networks
Checking cell 'AND_8bit{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.062 secs)
================================1586================================
Checking Wells and Substrates in 'ENGR338_Tucson:AND_8bit{lay}' ...
   Geometry collection found 312 well pieces, took 0.002 secs
   Geometry analysis used 6 threads and took 0.005 secs
NetValues propagation took 0.0 secs
Checking short circuits in 32 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.008 secs)
================================1587================================
Hierarchical NCC every cell in the design: cell 'AND_8bit{sch}'  cell 'AND_8bit{lay}'
Comparing: ENGR338_Tucson:AND{sch} with: ENGR338_Tucson:AND{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338_Tucson:AND_8bit{sch} with: ENGR338_Tucson:AND_8bit{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.005 seconds.
```



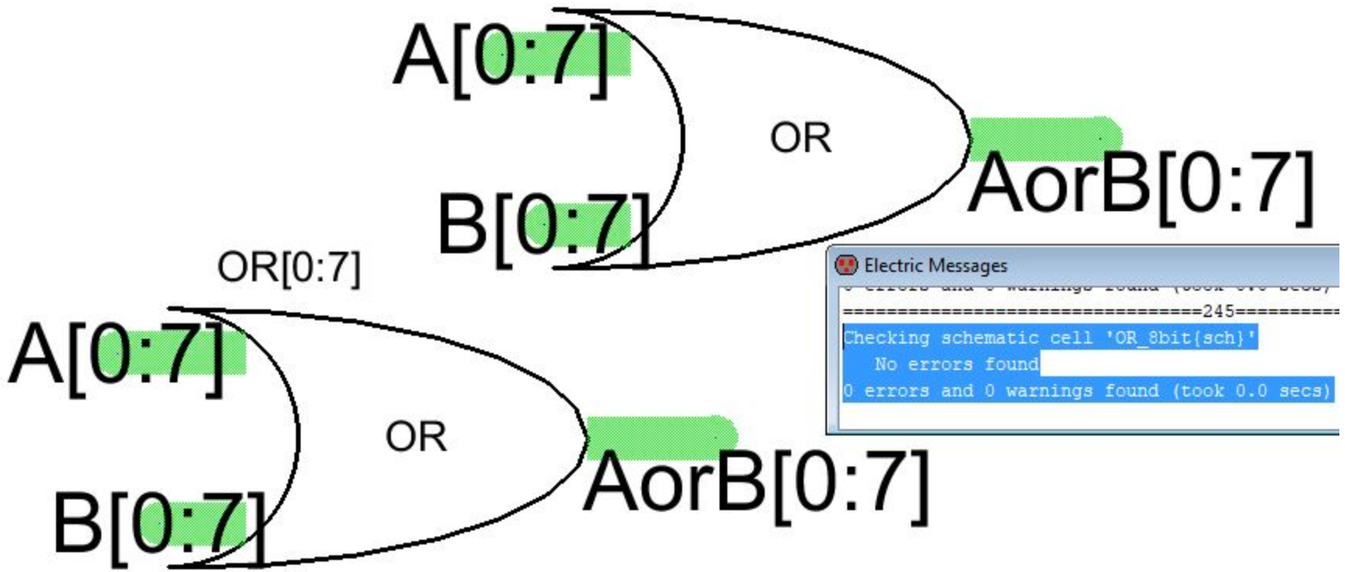

```
Checking schematic cell 'OR{sch}'
   No errors found
0 errors and 0 warnings found (took 0.003 secs)
```

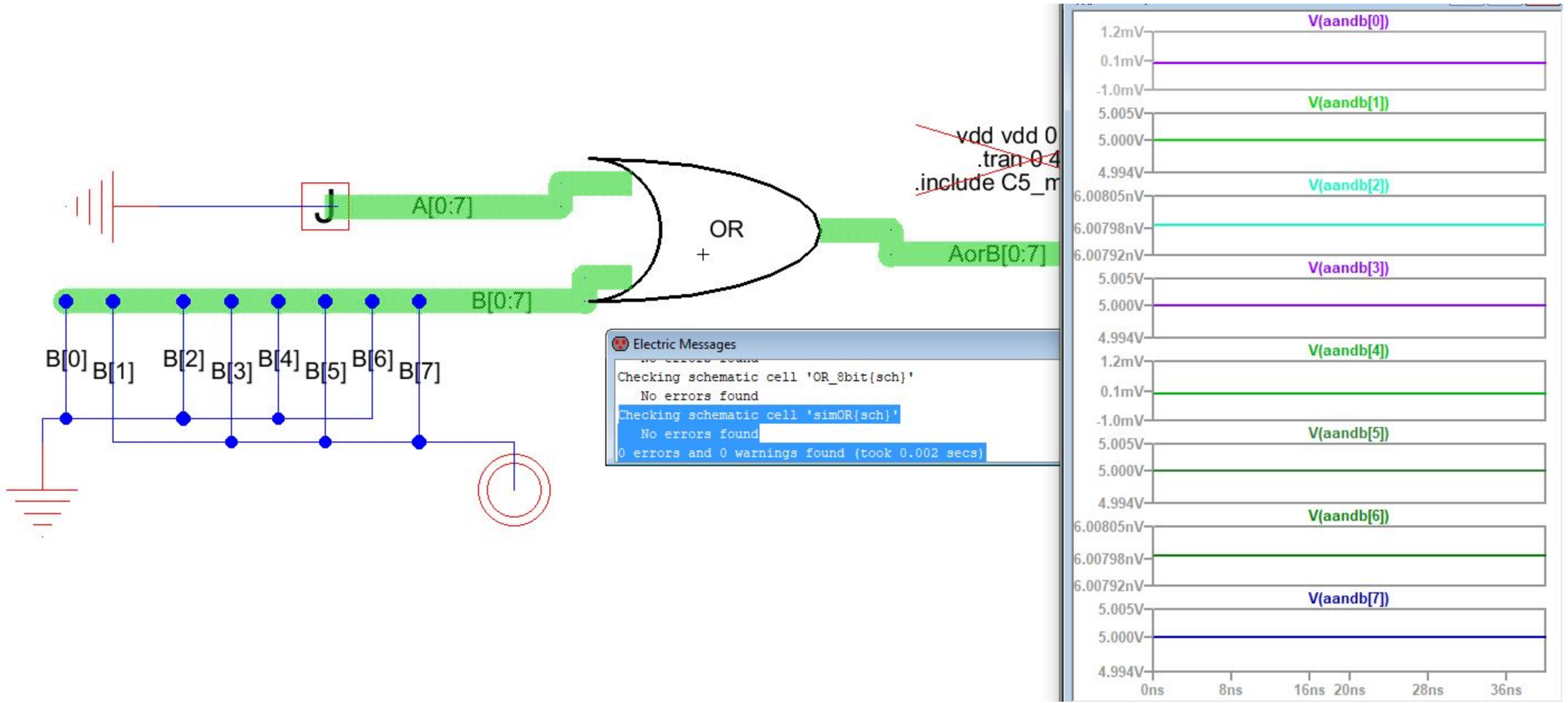

A
B
OR
AorB
vdd vdd 0 dc 5
vA A 0 PULSE(0 5 5n 10p 10p 10n 21n)
vB B 0 PULSE(0 5 10n 10p 10p 10n 21n)
.tran 0 40n
.include C5_models.txt
Electric Messages
==========55==========
Wiring added: 1 wire arc and 1 Wire_Pin node
==========56==========
Checking schematic cell 'OR{sch}'
No errors found
Checking schematic cell 'simNORNEW{sch}'
No errors found
0 errors and 0 warnings found (took 0.002 secs)
==========57==========
simNORNEW.spi
simNORNEW.spi
simNORNEW.spi
V(a)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
V(b)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
V(aorb)
5.4V
4.2V
3.0V
1.8V
0.6V
-0.6V
0ns
4ns
8ns
12ns
16ns
20ns
24ns
28ns
32ns
36ns
40ns

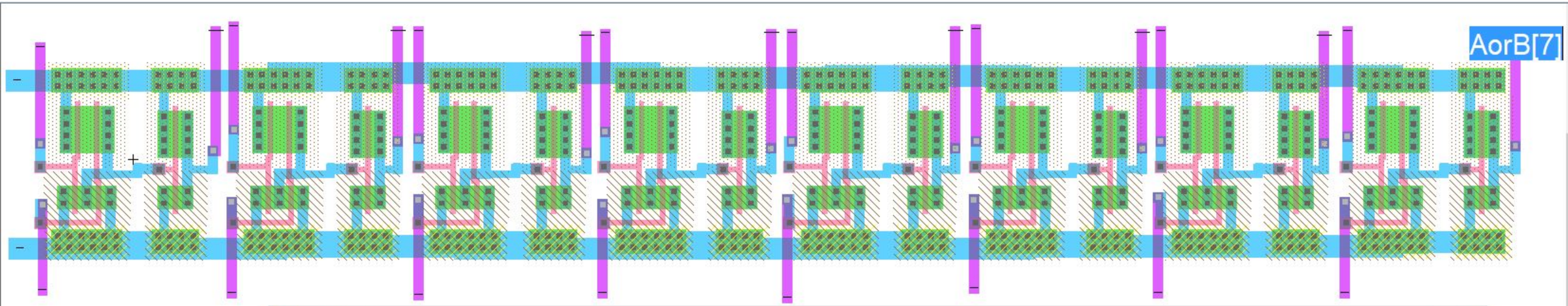


Electric Messages

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
Checking cell 'OR{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.018 secs)
================================90================================
Checking Wells and Substrates in 'ENGR338_Tucson:OR{lay}' ...
   Geometry collection found 30 well pieces, took 0.001 secs
   Geometry analysis used 6 threads and took 0.002 secs
NetValues propagation took 0.001 secs
Checking short circuits in 4 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.004 secs)
================================91================================
Hierarchical NCC every cell in the design: cell 'OR{sch}'  cell 'OR{lay}'
Comparing: ENGR338_Tucson:OR{sch} with: ENGR338_Tucson:OR{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.003 seconds.
```

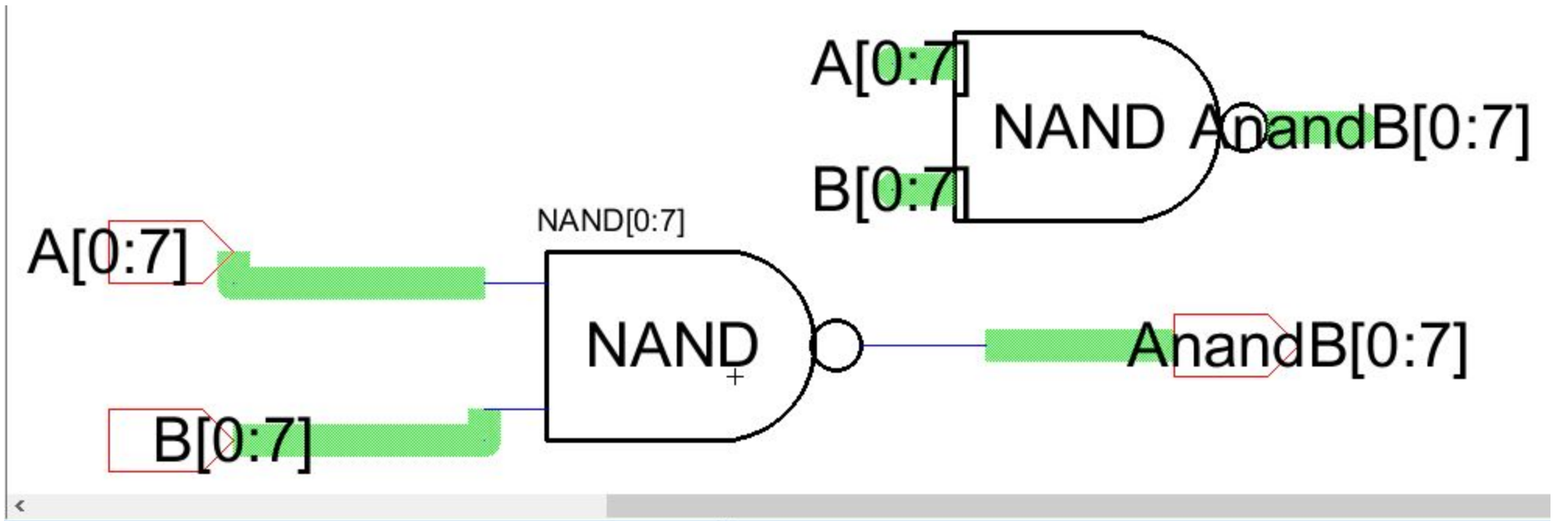

A[0:7]
B[0:7]
OR
AorB[0:7]
OR[0:7]
A[0:7]
B[0:7]
OR
AorB[0:7]
Electric Messages
==========245==========
Checking schematic cell 'OR_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)

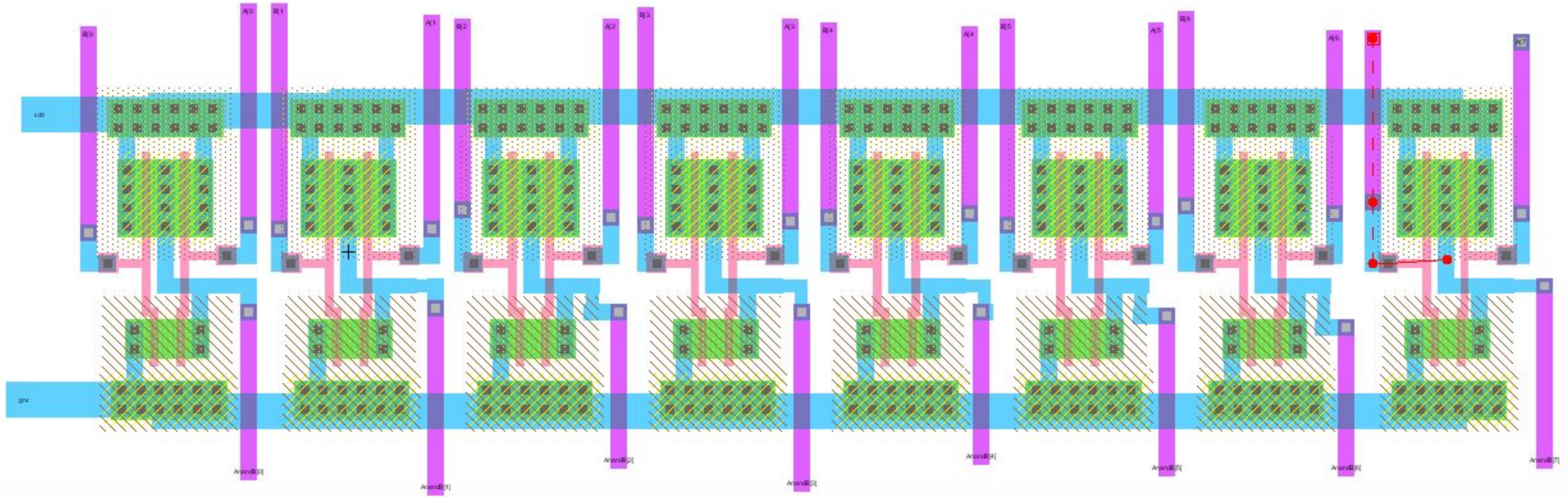

J
A[0:7]
B[0:7]
OR
AorB[0:7]
B[0] B[1] B[2] B[3] B[4] B[5] B[6] B[7]
vdd vdd 0
.tran 0 4
.include C5_m
Electric Messages
Checking schematic cell 'OR_8bit{sch}'
No errors found
Checking schematic cell 'simOR{sch}'
No errors found
0 errors and 0 warnings found (took 0.002 secs)
V(aandb[0])
1.2mV
0.1mV
-1.0mV
V(aandb[1])
5.005V
5.000V
4.994V
V(aandb[2])
6.00805nV
6.00798nV
6.00792nV
V(aandb[3])
5.005V
5.000V
4.994V
V(aandb[4])
1.2mV
0.1mV
-1.0mV
V(aandb[5])
5.005V
5.000V
4.994V
V(aandb[6])
6.00805nV
6.00798nV
6.00792nV
V(aandb[7])
5.005V
5.000V
4.994V
0ns
8ns
16ns
20ns
28ns
36ns



Electric Messages

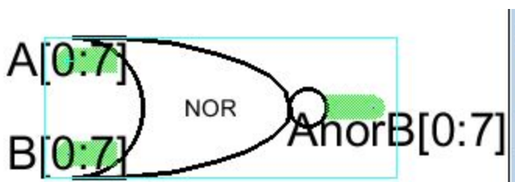
```
Checking again hierarchy .... (0.0 secs)
Found 27 networks
Checking cell 'OR_8bit{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.018 secs)
================================496================================
Checking Wells and Substrates in 'ENGR338_Tucson:OR_8bit{lay}' ...
   Geometry collection found 240 well pieces, took 0.001 secs
   Geometry analysis used 6 threads and took 0.002 secs
NetValues propagation took 0.001 secs
Checking short circuits in 32 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.005 secs)
================================497================================
Hierarchical NCC every cell in the design: cell 'OR_8bit{sch}'  cell 'OR_8bit{lay}'
Comparing: ENGR338_Tucson:OR{sch} with: ENGR338_Tucson:OR{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338_Tucson:OR_8bit{sch} with: ENGR338_Tucson:OR_8bit{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.003 seconds.
```


A[0:7]
NAND AnandB[0:7]
B[0:7]
NAND[0:7]
A[0:7]
NAND
AnandB[0:7]
B[0:7]
Checking schematic cell 'NAND{sch}'
No errors found
Checking schematic cell 'NAND_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.002 secs)

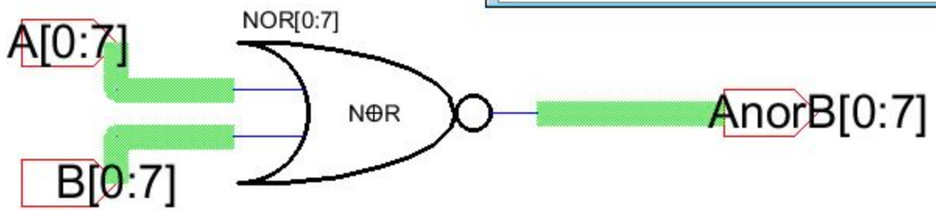


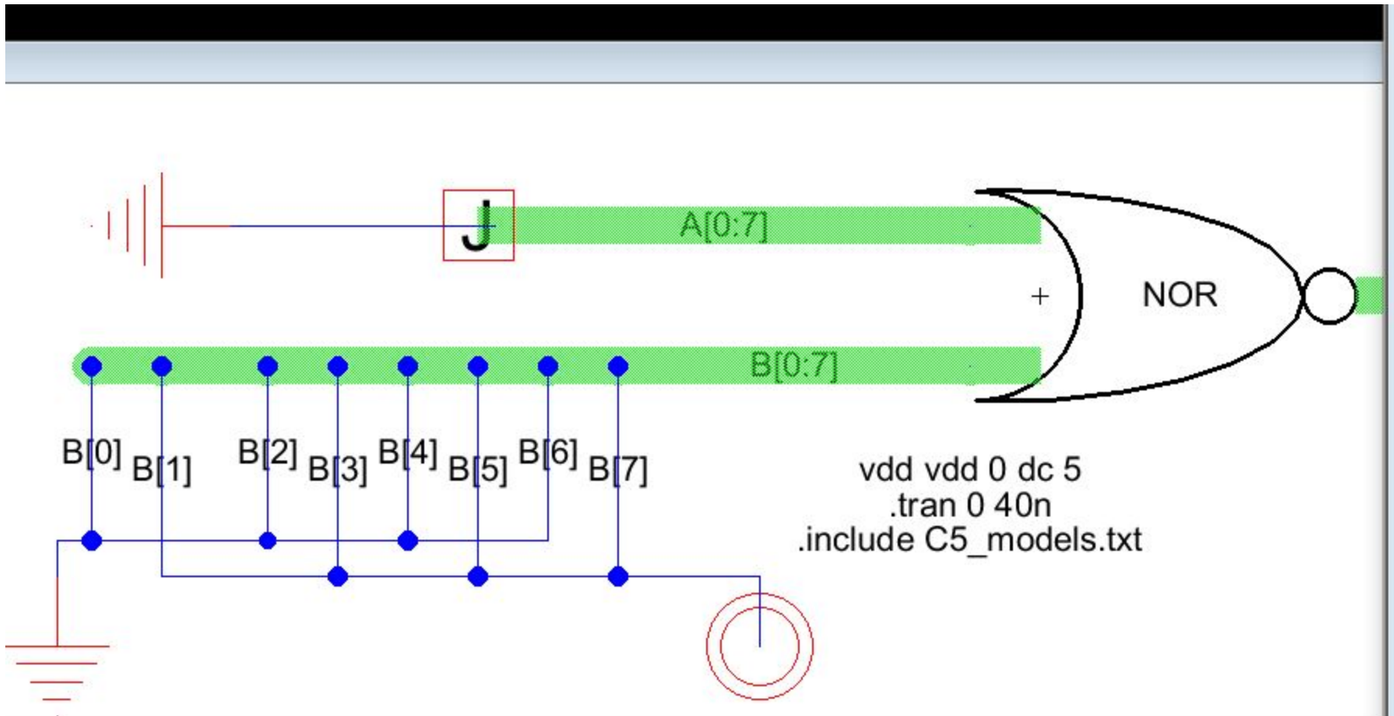
Electric Messages

```
Checking cell 'NAND_8bit{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.033 secs)
================================644================================
Checking Wells and Substrates in 'ENGR338_Tucson:NAND_8bit{lay}' ...
   Geometry collection found 144 well pieces, took 0.001 secs
   Geometry analysis used 6 threads and took 0.001 secs
NetValues propagation took 0.0 secs
Checking short circuits in 16 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.003 secs)
================================645================================
Hierarchical NCC every cell in the design: cell 'NAND_8bit{sch}'  cell 'NAND_8bit{lay}'
Comparing: ENGR338_Tucson:NAND{sch} with: ENGR338_Tucson:NAND{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: ENGR338_Tucson:NAND_8bit{sch} with: ENGR338_Tucson:NAND_8bit{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.005 seconds.
```



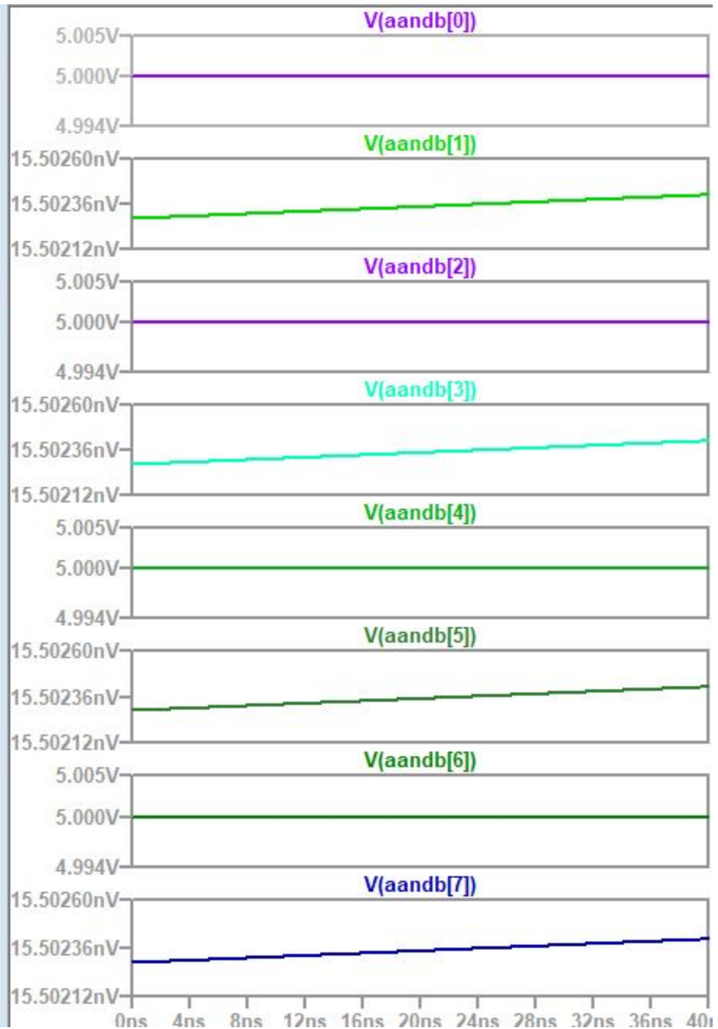

```
==================================23==============
Checking schematic cell 'NOR{sch}'
   No errors found
Checking schematic cell 'NOR_8bit{sch}'
   No errors found
0 errors and 0 warnings found (took 0.001 secs)
```

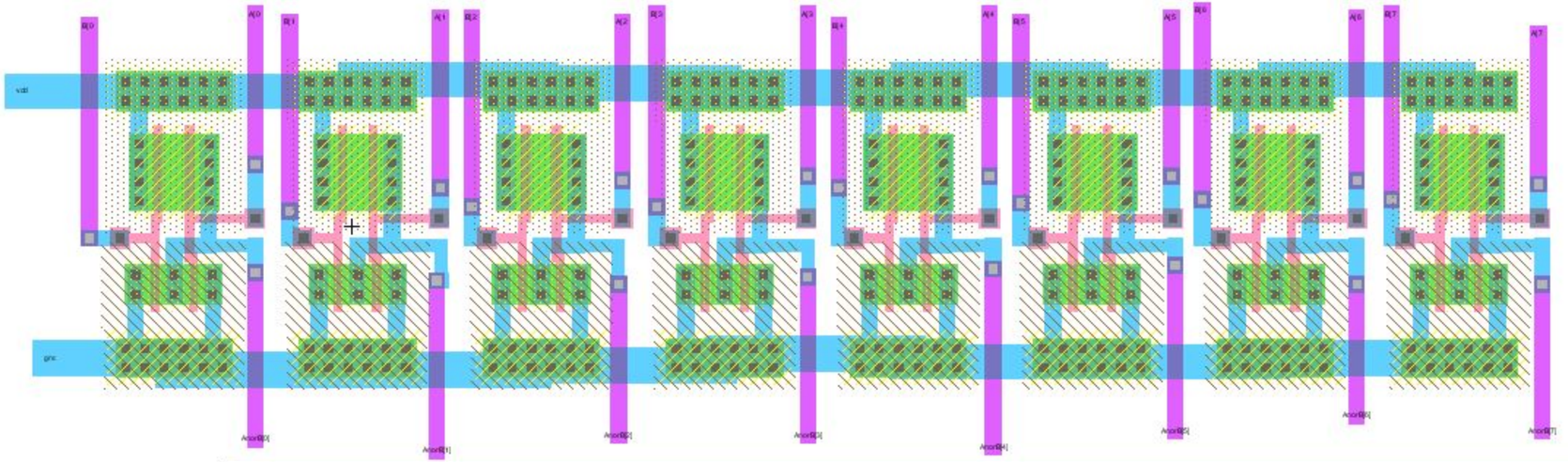




Electric Messages

```
================================27================================
Checking schematic cell 'NOR{sch}'
   No errors found
Checking schematic cell 'NOR_8bit{sch}'
   No errors found
Checking schematic cell 'simXOR_bus{sch}'
   No errors found
0 errors and 0 warnings found (took 0.002 secs)
================================28================================
```





Electric Messages

```
        No errors/warnings found
0 errors and 0 warnings found (took 0.026 secs)
================================193================================
Checking Wells and Substrates in 'ENGR338_Tucson:NOR_8bit{lay}' ...
   Geometry collection found 144 well pieces, took 0.001 secs
   Geometry analysis used 6 threads and took 0.002 secs
NetValues propagation took 0.0 secs
Checking short circuits in 16 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.003 secs)
================================194================================
Hierarchical NCC every cell in the design: cell 'NOR_8bit{sch}'  cell 'NOR_8bit{lay}'
Comparing: ENGR338_Tucson:NOR{sch} with: ENGR338_Tucson:NOR{lay}
  exports match, topologies match, sizes not checked in 0.022 seconds.
Comparing: ENGR338_Tucson:NOR_8bit{sch} with: ENGR338_Tucson:NOR_8bit{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.03 seconds.
```