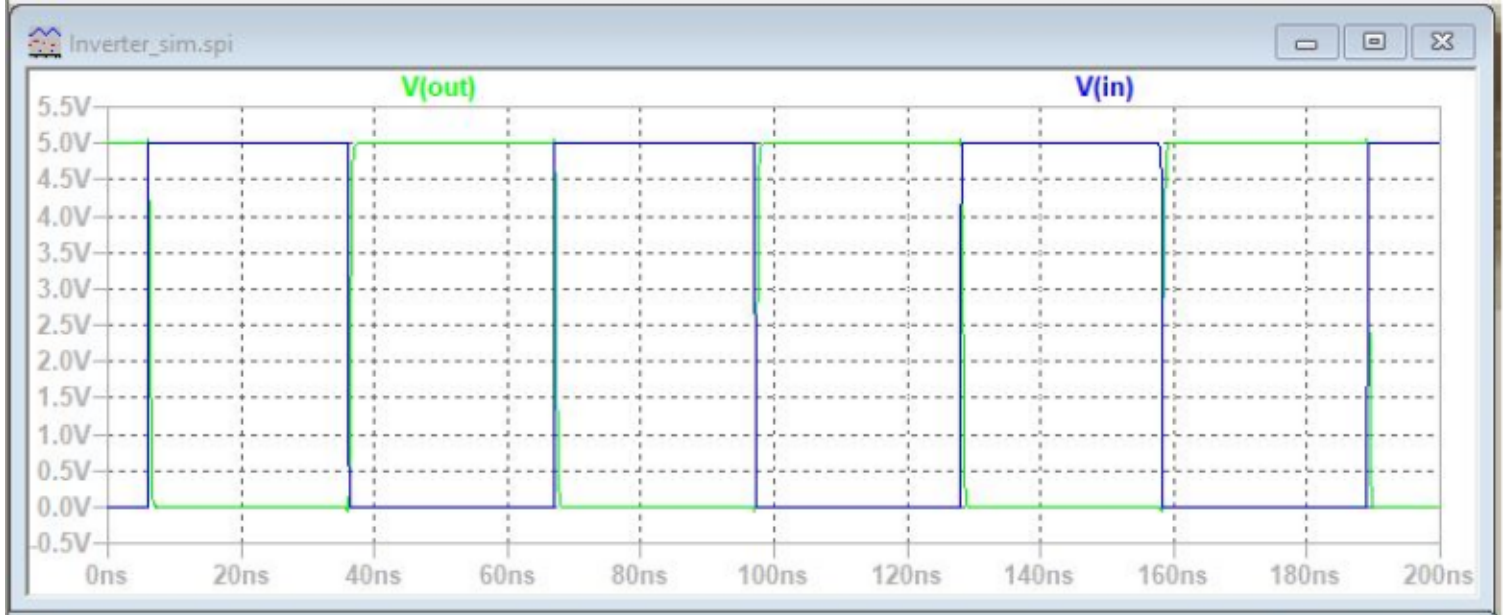
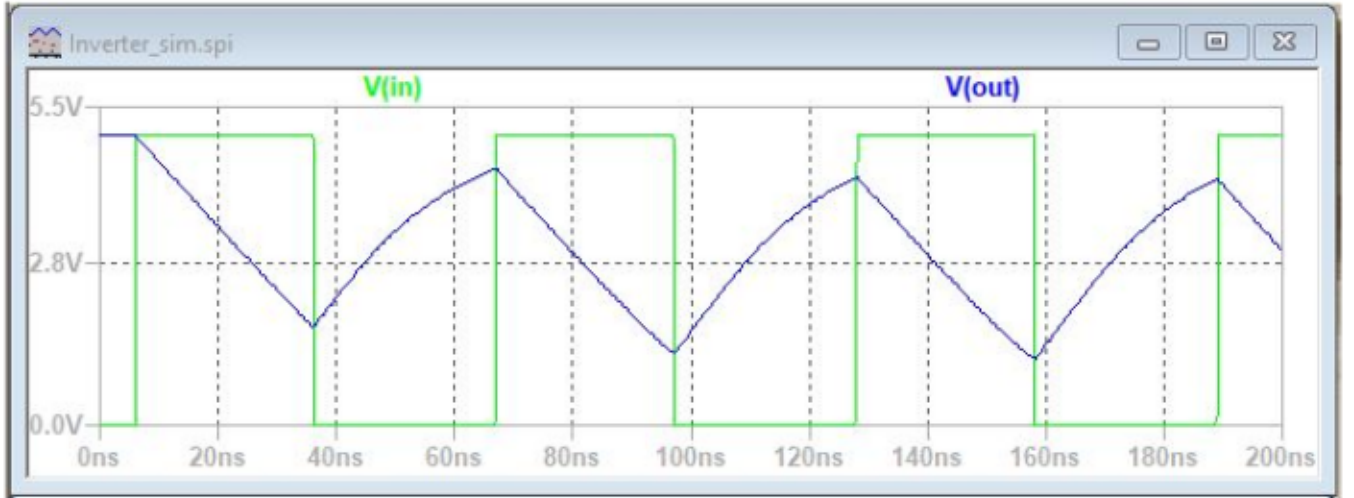


Inverter_sim.spi

```
* Spice Code nodes in cell cell 'Inverter_sim{sch}'
vdd vdd 0 DC 5
vin in 0 PULSE(0 5 6n 100p 100p 30n 61n)
.tran 200n
.options plotwinsize=0
.include C5_models.txt
.END
```

erter_sim.spi

```
nos-4@0 out in vdd pmos-4@0_b PMOS L=0.6U W=6U

Spice Code nodes in cell cell 'Inverter_sim{sch}'
d vdd 0 DC 5
n in 0 PULSE(0 5 6n 100p 100p 30n 61n)
tan 200n
ptions plotwinsize=0
nclude C5_models.txt
ND
```



Inverter_sim.spi

```
* Spice Code nodes in cell cell 'Inverter_sim{sch}'
vdd vdd 0 DC 5
vin in 0 PULSE(0 5 6n 100p 100p 30n 61n)
.tran 200n
.options plotwinsize=0
.include C5_models.txt
.END
```

Inverter_100_50_sim.spi

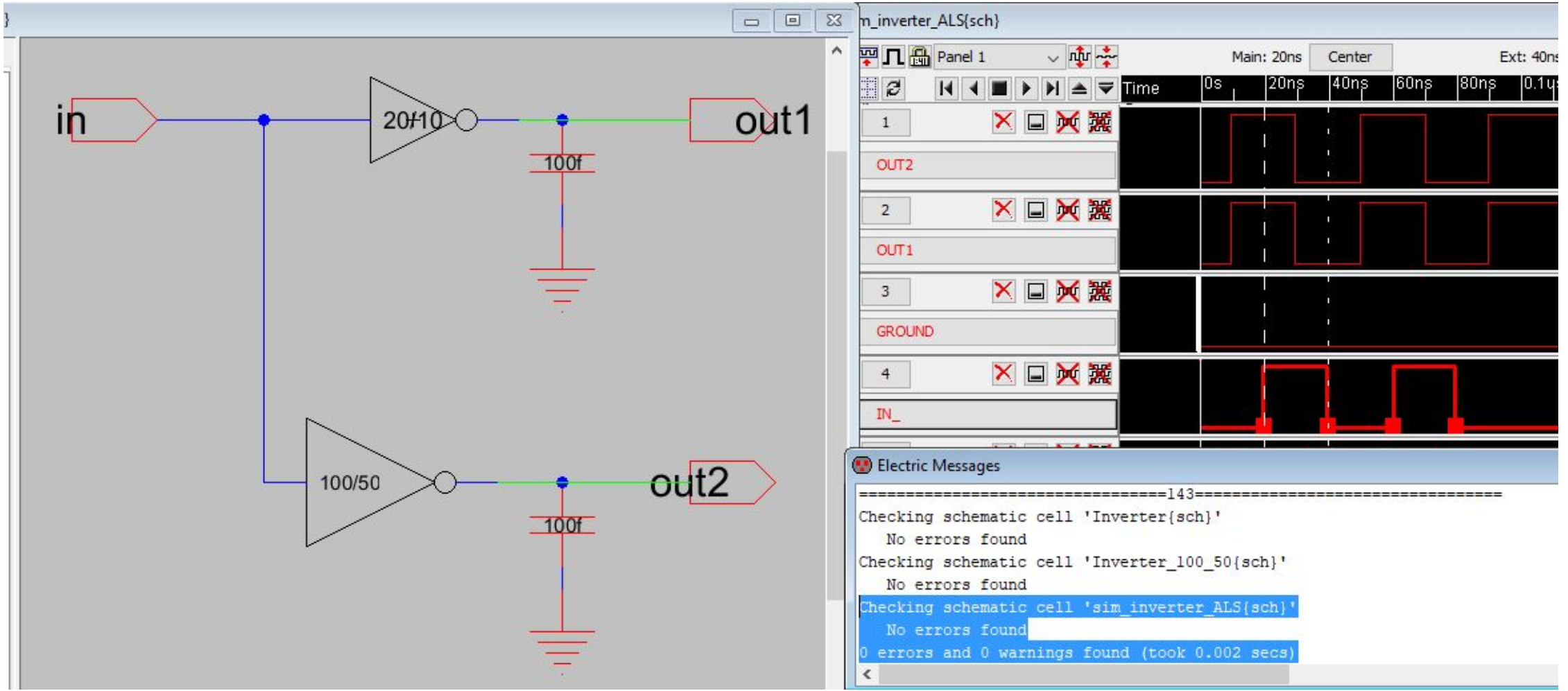
```
Mnmos@0 out in gnd gnd NMOS L=0.6U W=3U M=5
Mpmos-4@0 out in vdd pmos-4@0_b PMOS L=0.6U W=6U M=5

* Spice Code nodes in cell cell 'Inverter_100_50_sim{sch}'
vdd vdd 0 DC 5
vin in 0 PULSE(0 5 6n 100p 100p 30n 61n)
.tran 200n
.options plotwinsize=0
.include C5_models.txt
.END
```

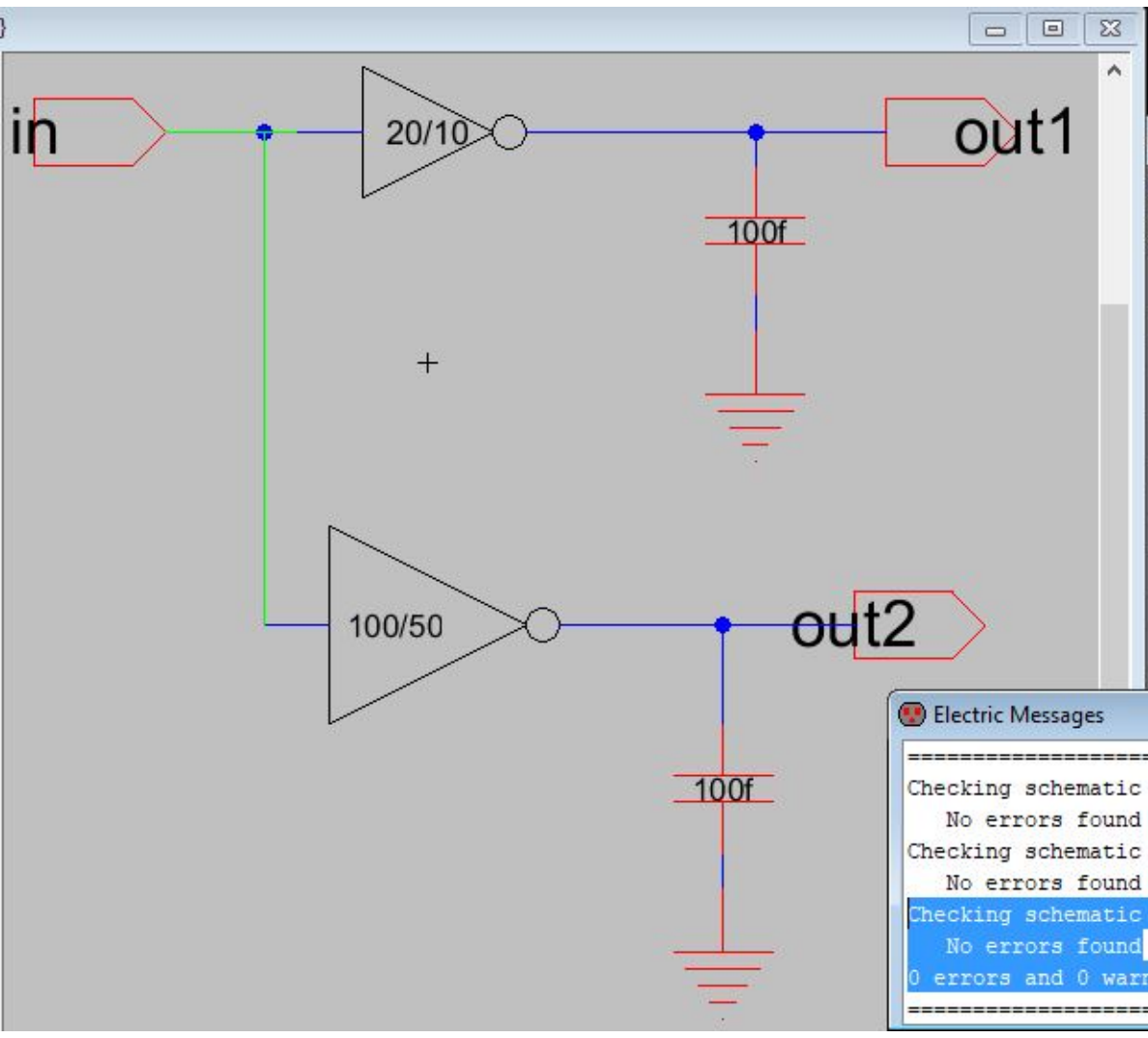
50_sim.spi

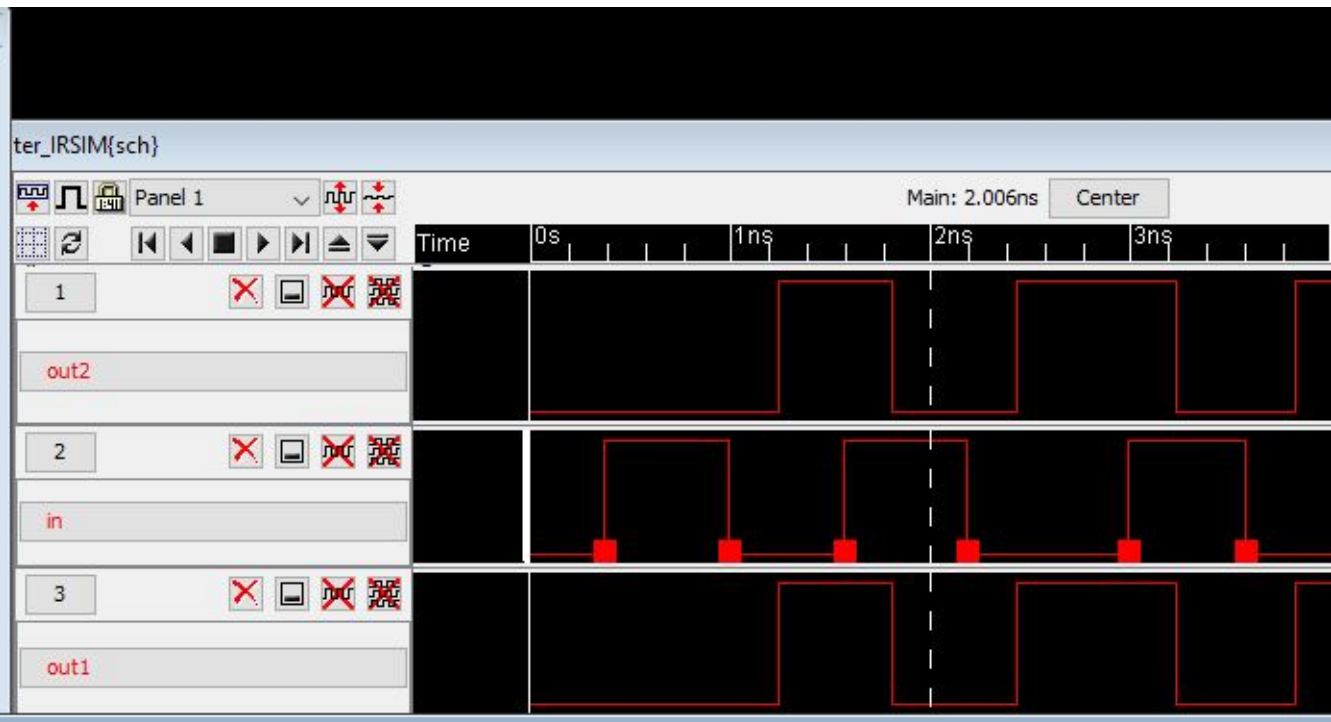
```
out in gnd gnd NMOS L=0.6U W=3U M=5
0 out in vdd pmos-4@0_b PMOS L=0.6U W=6U M=5

Code nodes in cell cell 'Inverter_100_50_sim{sch}'
0 DC 5
 PULSE(0 5 6n 100p 100p 30n 61n)
0n
 plotwinsize=0
 C5_models.txt
```

0_50_sim.spi

```
) out in gnd gnd NMOS L=0.6U W=3U M=5
:@0 out in vdd pmos-4@0_b PMOS L=0.6U W=6U M=5

: Code nodes in cell cell 'Inverter_100_50_sim{sch}'
{ 0 DC 5
 0 PULSE(0 5 6n 100p 100p 30n 61n)
:00n
ıs plotwinsize=0
le C5_models.txt
```


in
20/10
100f
out1
100/50
100f
out2
m_inverter_ALS{sch}
Panel 1
Main: 20ns
Center
Ext: 40ns
Time
0s
20ns
40ns
60ns
80ns
1
OUT2
2
OUT1
3
GROUND
4
IN_
Electric Messages
==========143==========
Checking schematic cell 'Inverter{sch}'
No errors found
Checking schematic cell 'Inverter_100_50{sch}'
No errors found
Checking schematic cell 'sim_inverter_ALS{sch}'
No errors found
0 errors and 0 warnings found (took 0.002 secs)





Electric Messages

```
==================================10==================================
Checking schematic cell 'Inverter{sch}'
   No errors found
Checking schematic cell 'Inverter_100_50{sch}'
   No errors found
Checking schematic cell 'sim_inverter_IRSIM{sch}'
   No errors found
0 errors and 0 warnings found (took 0.003 secs)
==================================11==================================
```