

Lab 7 Using Buses in ElectricVLSI

Calvin Reese
cjreese@fortlewis.edu

10/24/2021

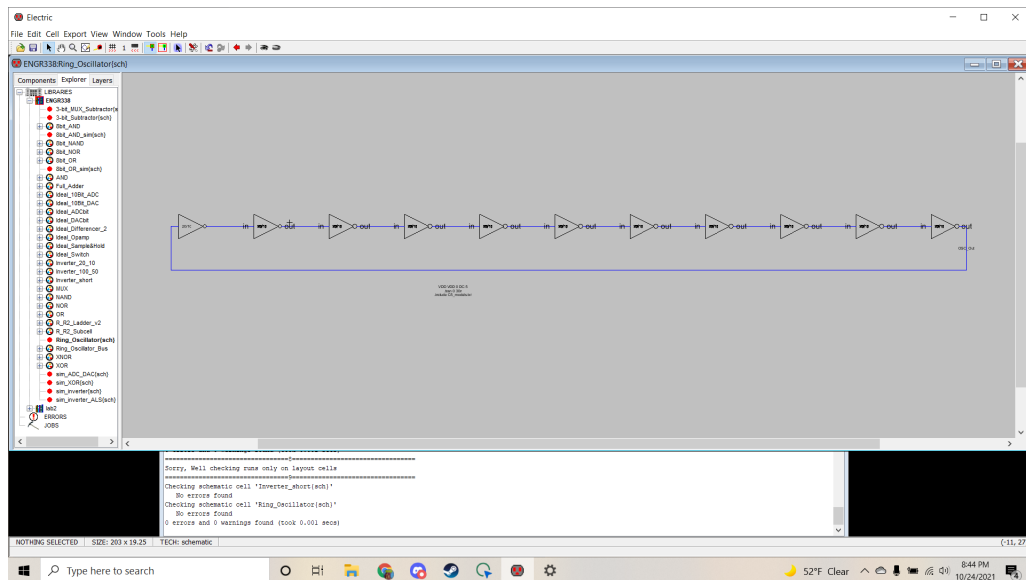
1 Introduction

This report will go over the process of making busses in ElectricVLSI.

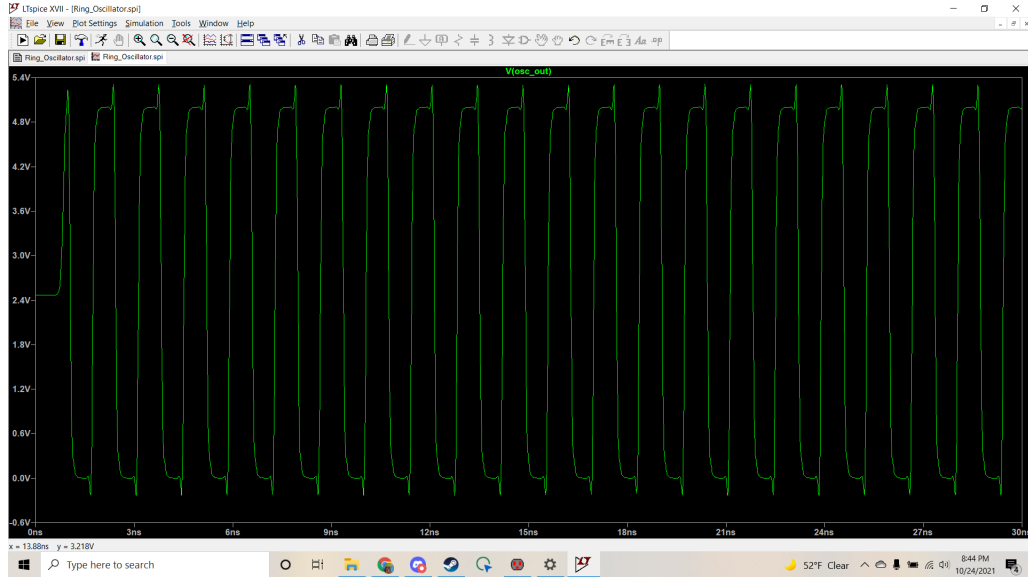
2 Materials and Methods

Busses are denoted by the `[:]` after a name to indicate the number of times the inputs and outputs are repeated, starting at the first and ending with the second. The tutorial for making these exact example in ElectricVLSI are found in <http://www.yilectronics.com/Courses/ENGR338LCE/f2021/lab7TheBus/Lab7.html>.

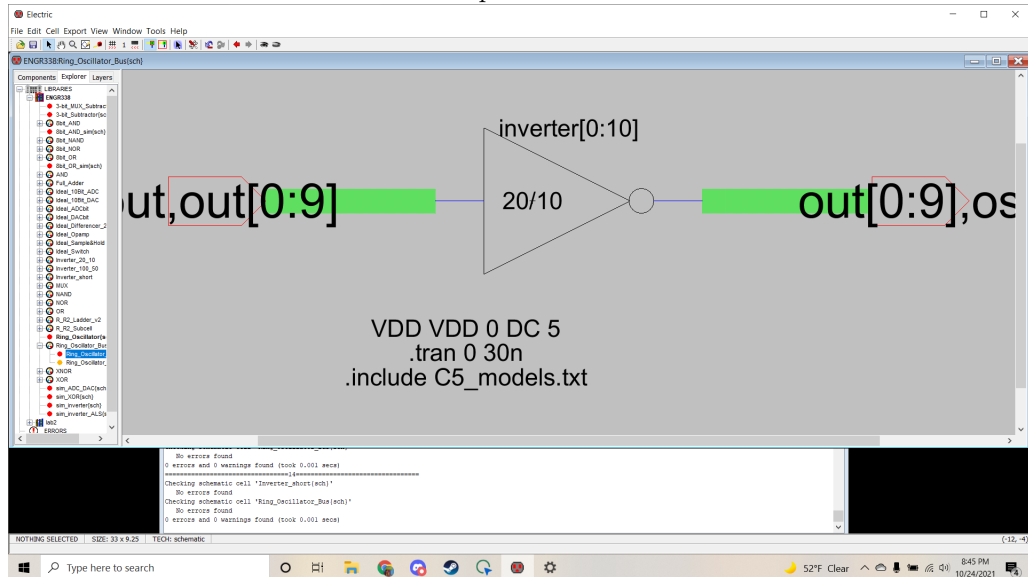
3 Results



Inverter Oscillator



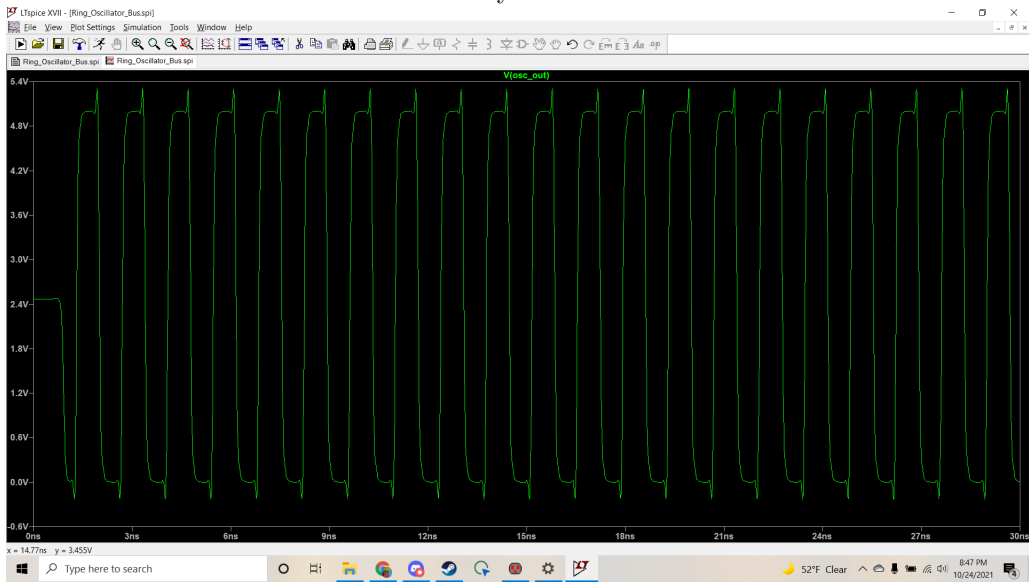
Inverter Oscillator Output



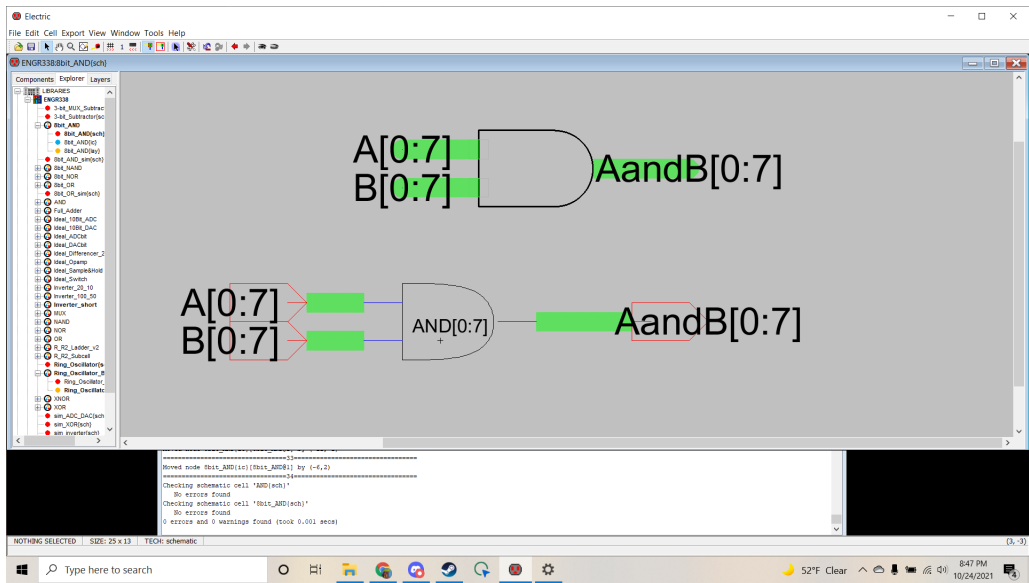
Bus Inverter Oscillator



Bus Inverter Oscillator Layout



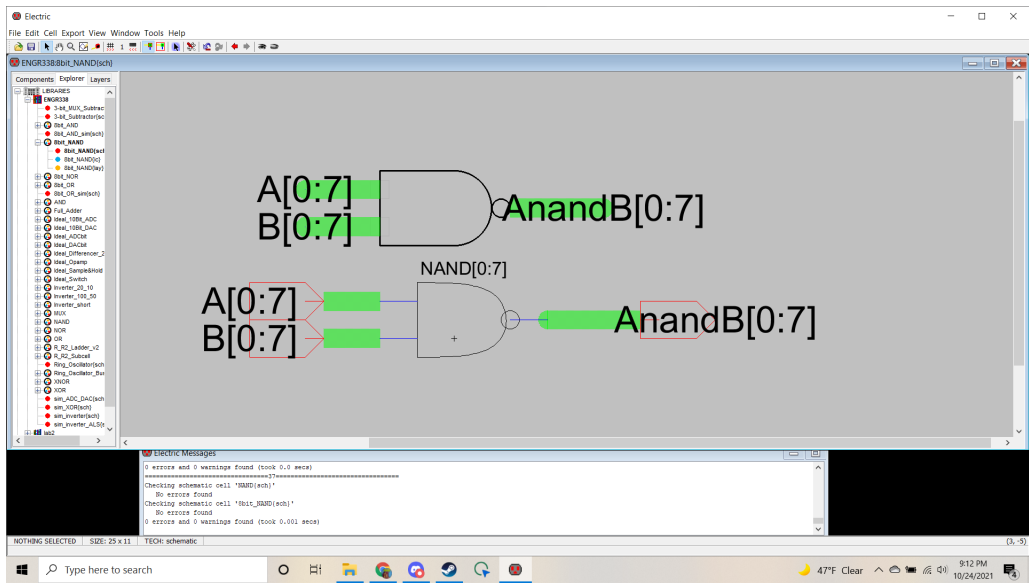
Bus Inverter Oscillator Output



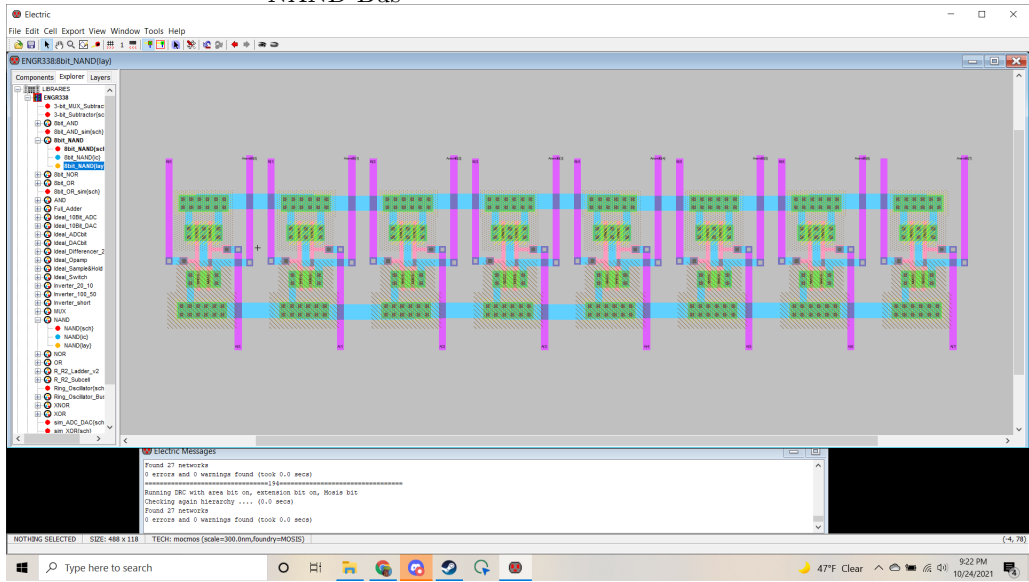
AND Bus



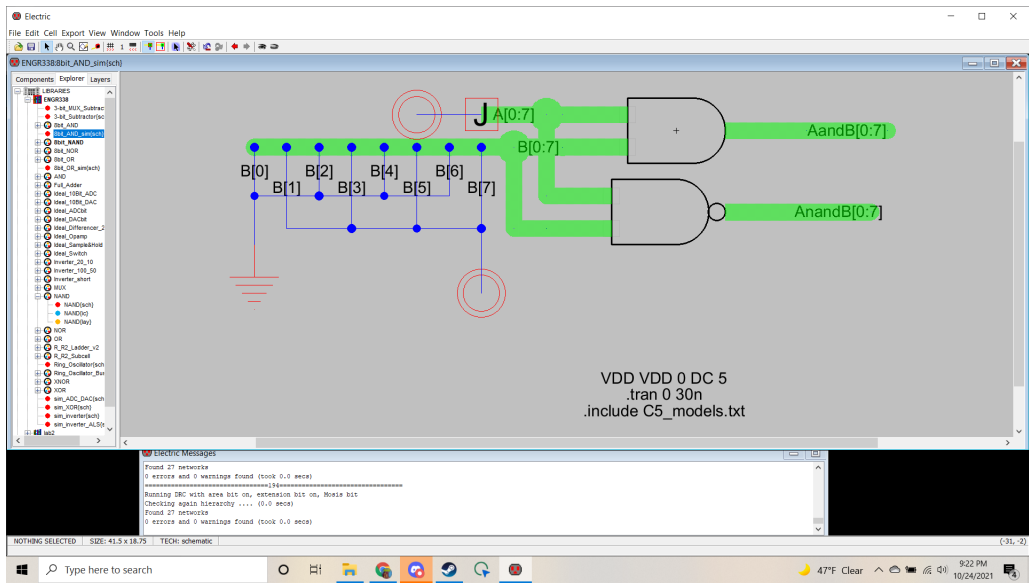
AND Bus Layout



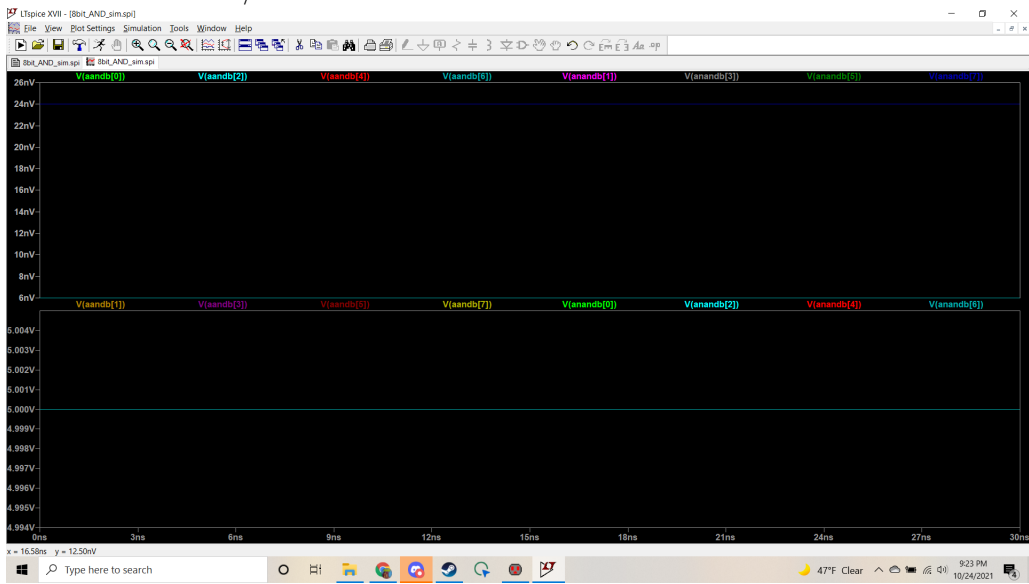
NAND Bus



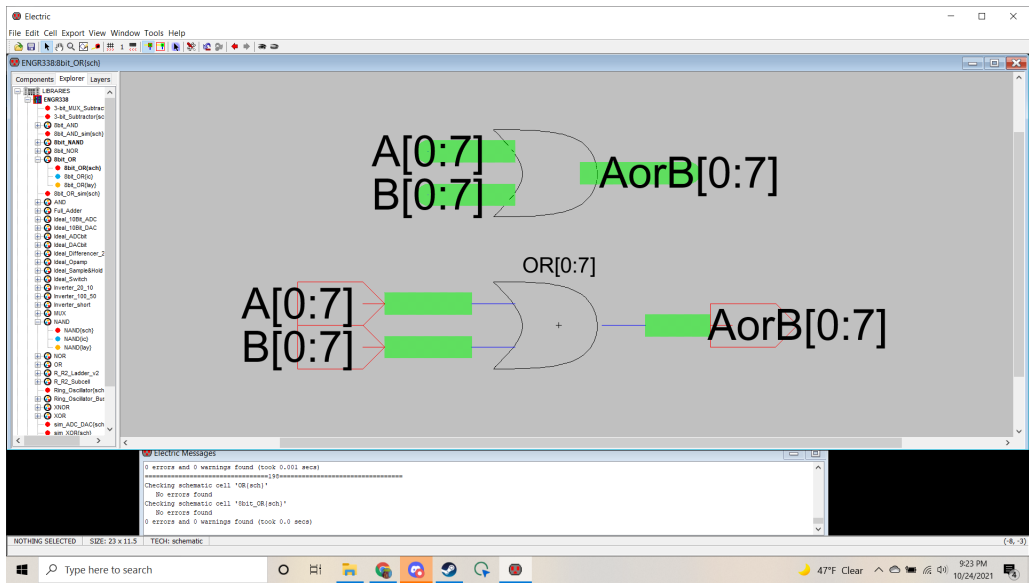
NAND Bus Layout



N/AND Bus Simulator



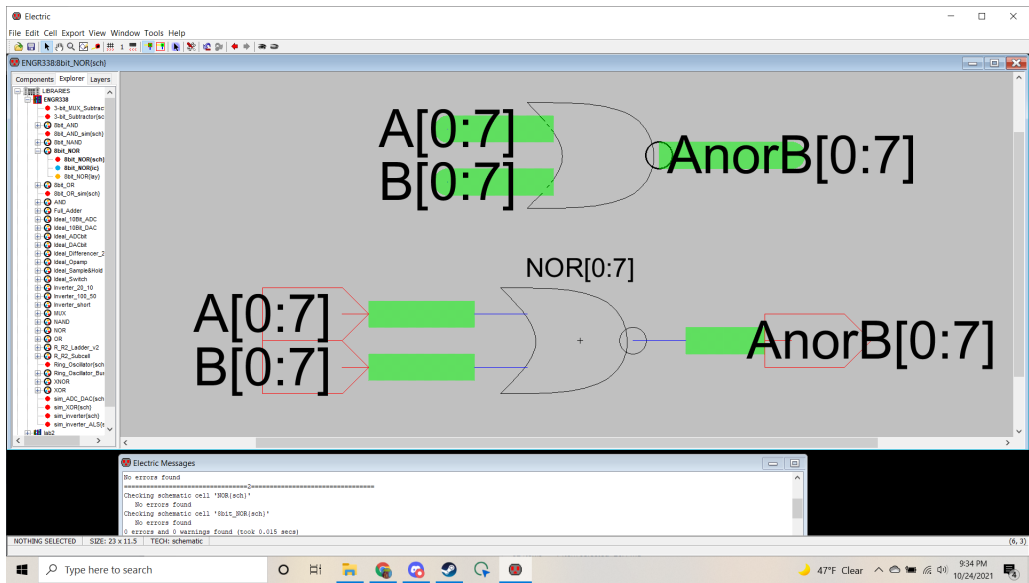
N/AND Bus Output



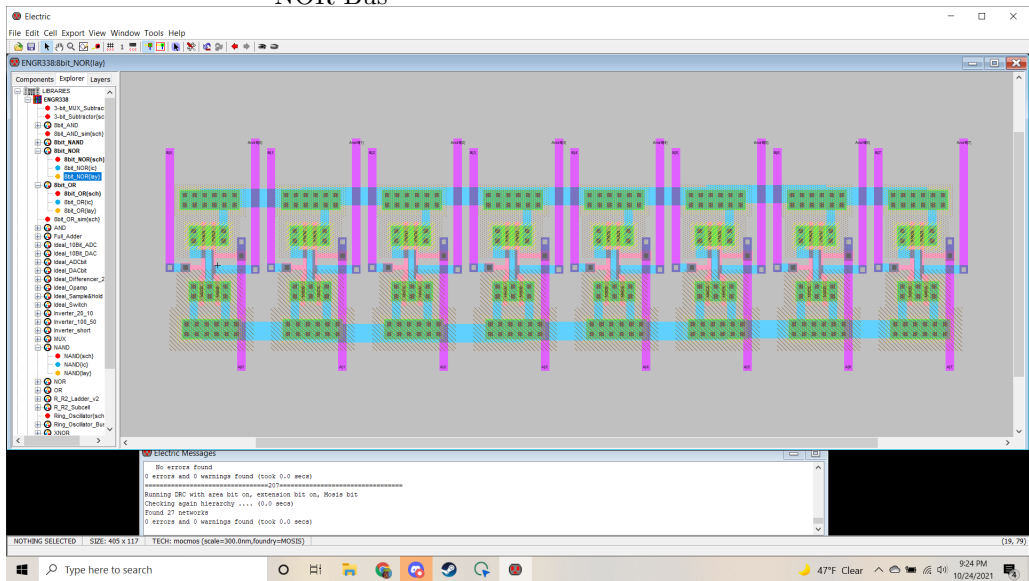
OR Bus



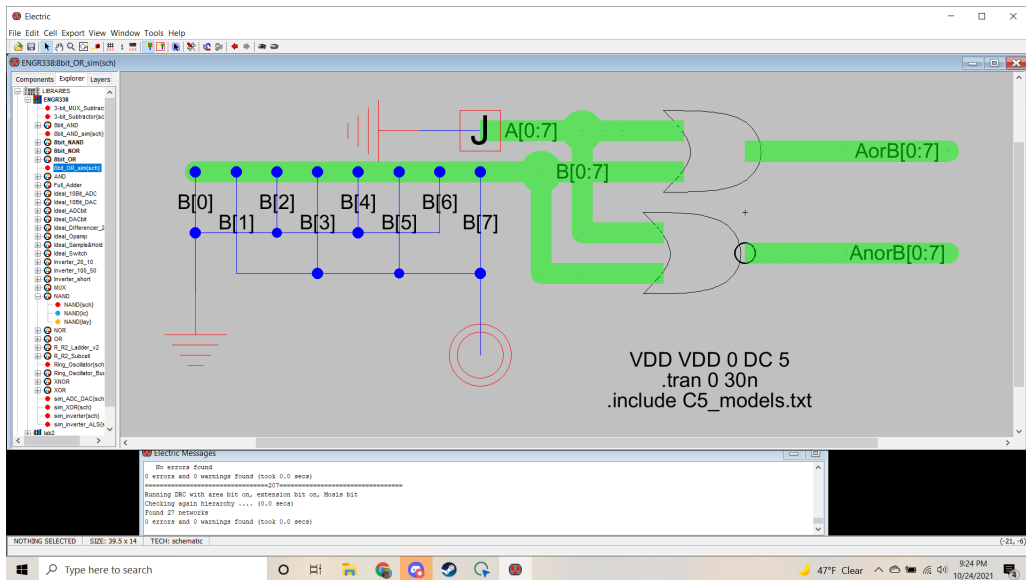
OR Bus layout



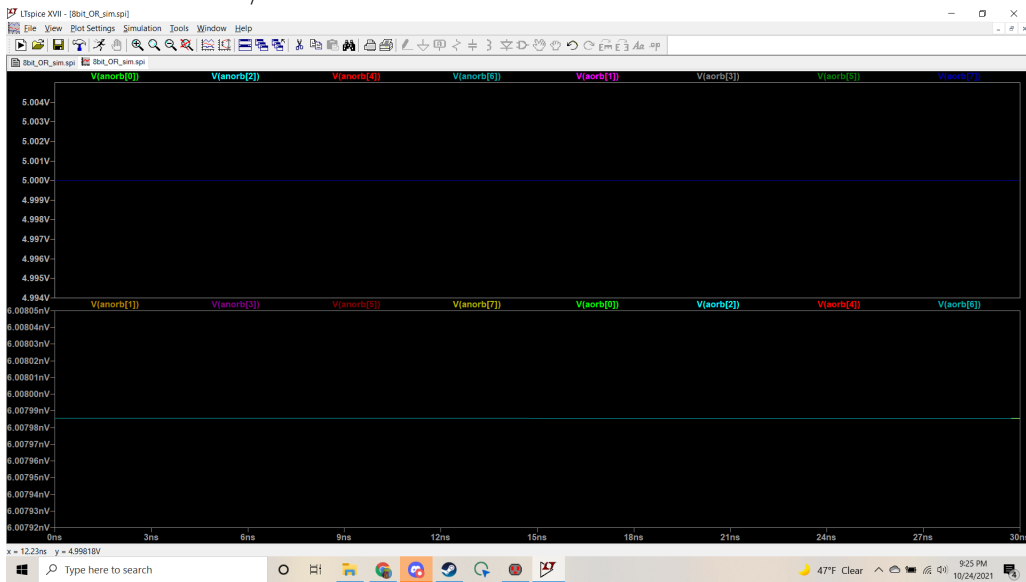
NOR Bus



NOR Bus layout



N/OR Bus Simulator



N/OR Bus Output

4 Discussion

As seen above, the outputs follow the inverter, N/AND and N/OR logics as intended in a bus format. Busses can be most useful when receiving multiple signals that all require the same function applied to it in an organized manner.