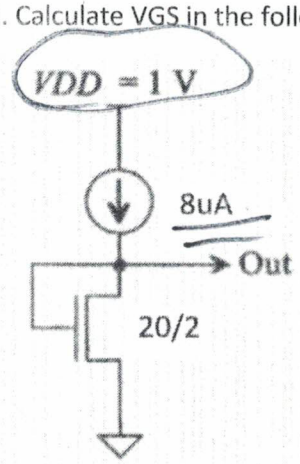
$V_{GS} = \sqrt{\frac{2I_{DS}}{\beta_n}} + V_{THN}$

CE338 Q7

1. Calculate VGS in the following circuit. KPn = 120 uA/v². (50 points)



$I_{DS} = \frac{K_{Pn}}{2}\frac{W}{L}(V_{GS}-V_{THN})^2$

$\beta_n = K_{Pn}\cdot\frac{W}{L} = 120\mu\cdot\frac{20}{2} = 1200\ \mu A/V^2$

$I_{DS} = \frac{\beta_n}{2}(V_{GS}-V_{THN})^2$

$2I_{DS} = \beta_n(V_{GS}-V_{THN})^2$

$\frac{2I_{DS}}{\beta_n} = (V_{GS}-V_{THN})^2 \Rightarrow \sqrt{\frac{2I_{DS}}{\beta_n}} = V_{GS}-V_{THN}$

$\Rightarrow V_{GS} = \sqrt{\frac{2I_{DS}}{\beta_n}} + V_{THN}$

$= \sqrt{\frac{16\ mA}{1200\ \mu A/V^2}} + 0.$

$= 0.115 + 0.$

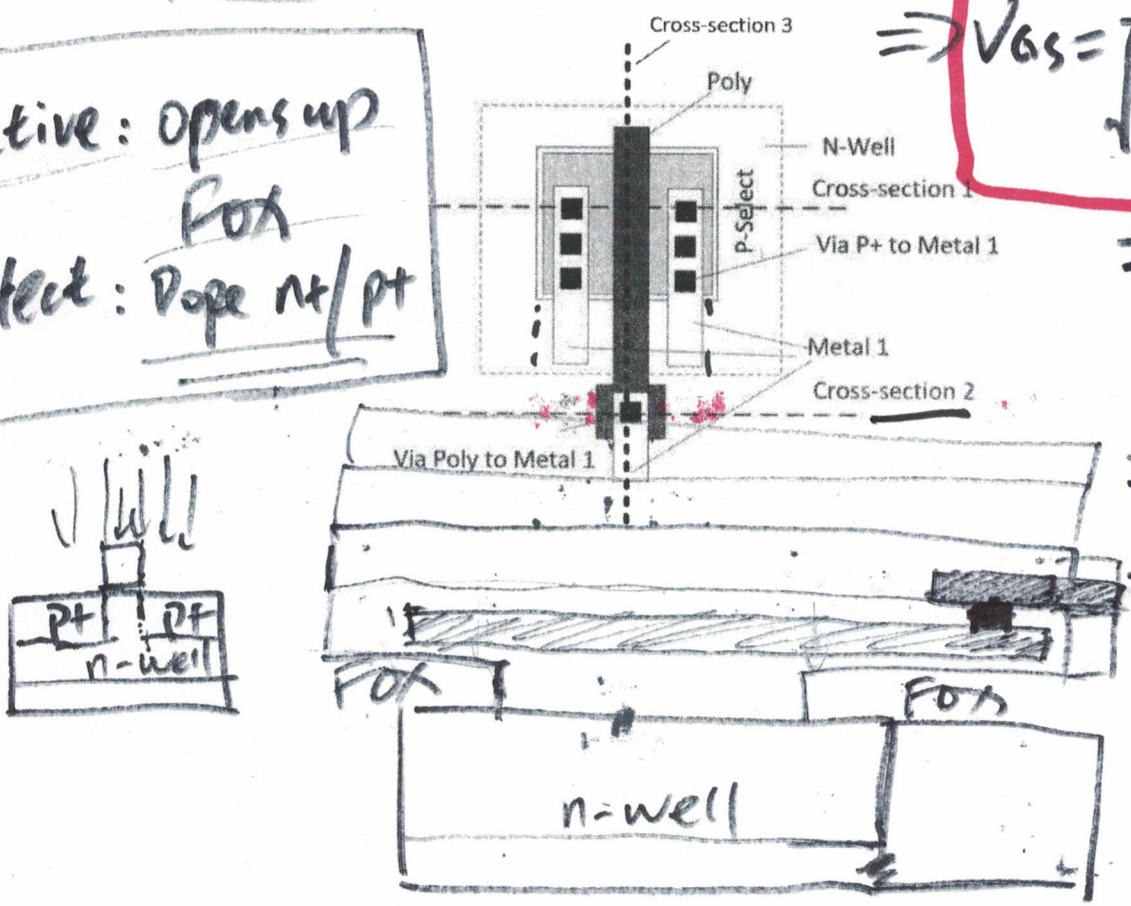
$= 0.915\ V$

2. Draw cross-section 3 for the following layout. (50 points)

Active: Opens up

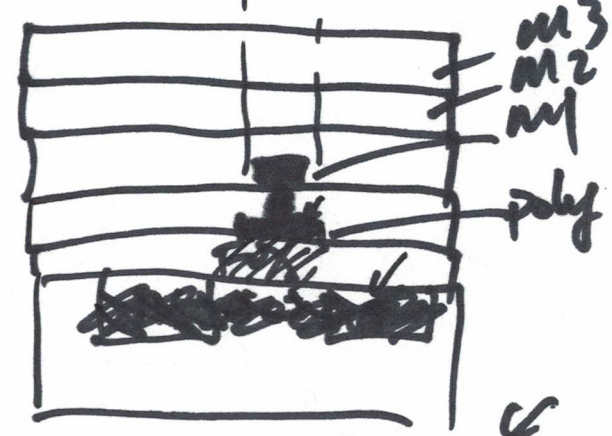
Fox

Select: Dope n+/p+

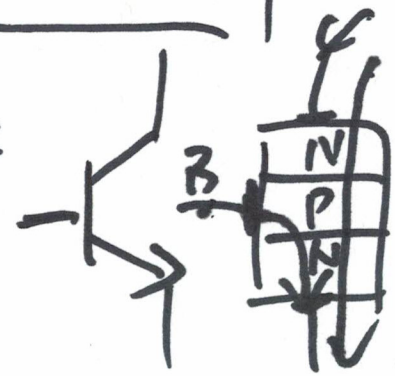


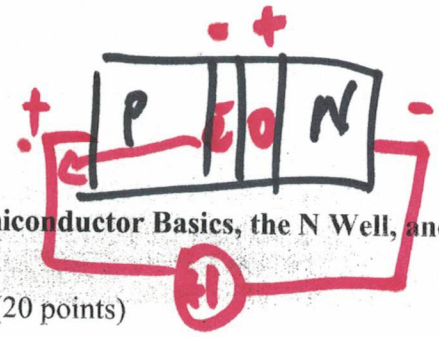
Bottom-up

CMOS



BJT





thinner

$C = \varepsilon \frac{A}{d_2} \uparrow$

ENGR338 HW 3 Semiconductor Basics, the N Well, and C5 Layers

1. Draw a pn junction and explain: (20 points)

1) Without an external voltage, the formation of a depletion region.

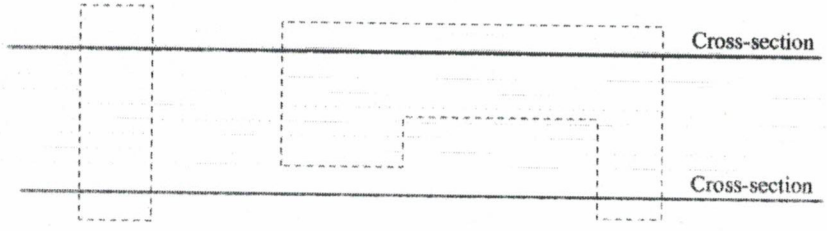
2) With an external voltage, explain the changes of the width of the depletion region under 'forward bias' and 'reverse bias' operations.

3) Explain how the depletion region will be changed, and how the diode capacitance will be changed with an increasing voltage under both 'forward bias' and 'reverse bias' operations.

4) Hand-draw the I-V curve of a real diode (with a 0.7 built-in voltage and no reverse breakdown) and the IV curve of an ideal diode.

5) Hand-draw the IV curve of a real Zener diode (with a 0.7 built-in voltage and a -Vz) and the IV curve of an ideal Zener diode.

2. For the layout of n-wells seen in the following figure (top view), sketch the cross-sectional views at the places indicated. Is there a parasitic pn junction in the layout? If so, where? (20 points)



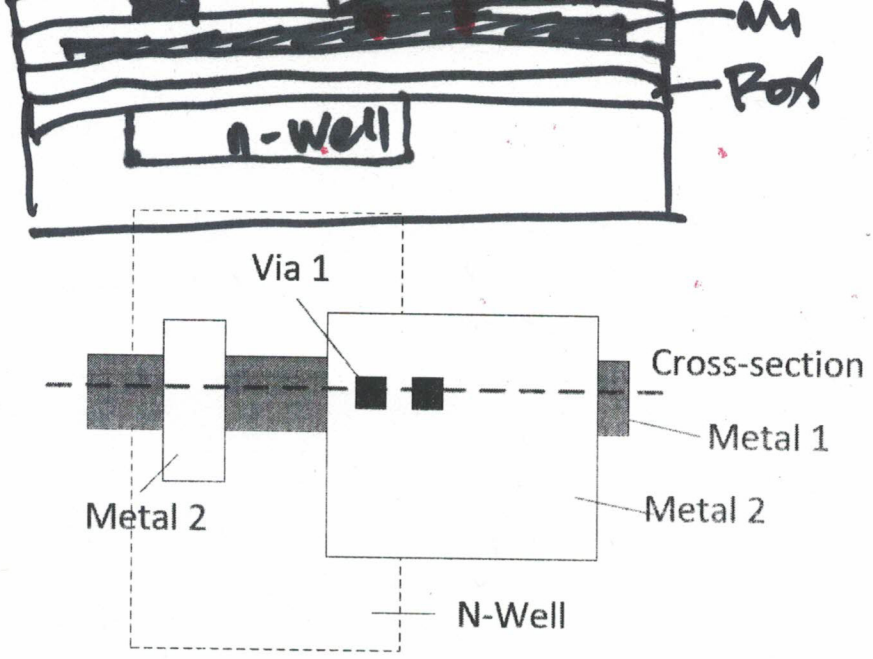
3. An n-well resistor has a width of 20 and a length of 400. A 20 by 20 square of n-well has a 15 fF parasitic capacitance. If the square resistance is 800 ohm, what is the time delay through this resistor without any extra load? (10 points)

4. The following figure shows the top-view of a layout. Draw the cross-sectional view of the location indicated by the dashed line. (10 points)

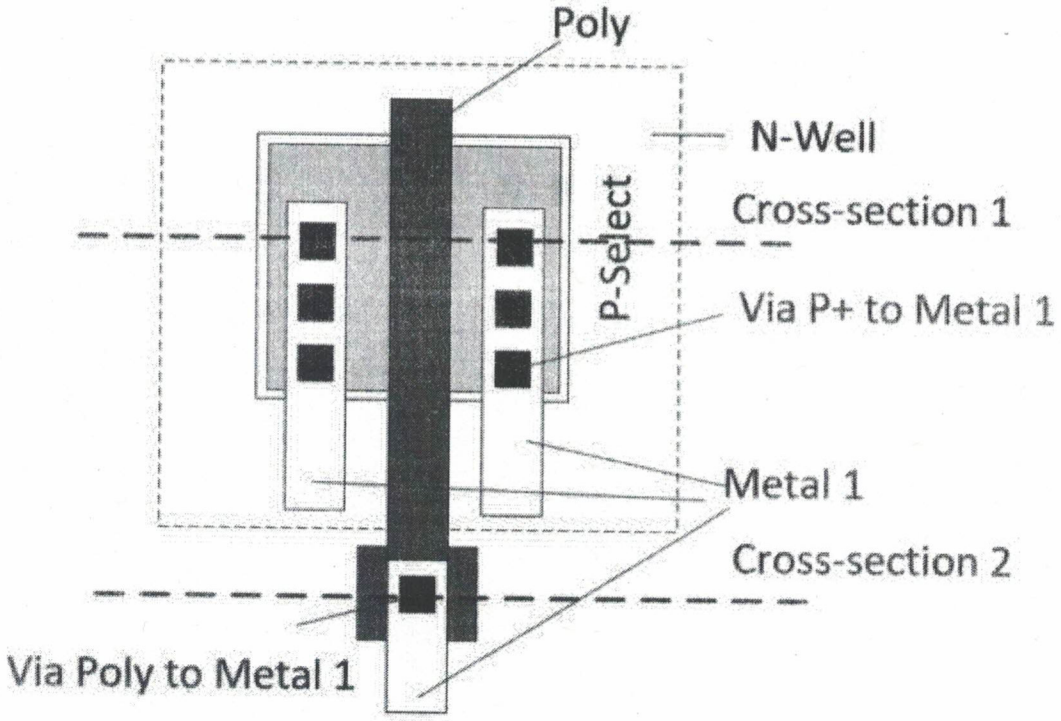
Distributed Time Delay

RC

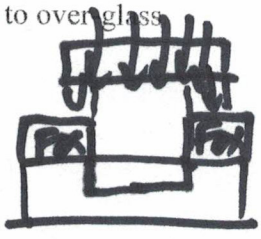
$0.35 \cdot R_{square} \cdot C_{square} \cdot L^2$



5. The following figure shows the top-view of a layout. Draw the cross-sectional views (cross-section 1 and cross-section 2 of the locations indicated by the dashed lines. (10 points)



6. Draw the cross-sectional view of all the layers of the C5 technology (from P-sub to overglass opening). (10 points)



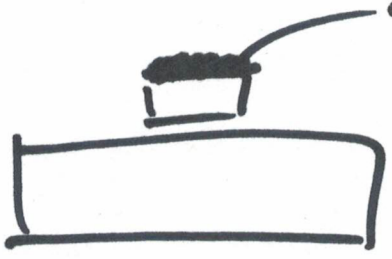
7. Why the footprint of N-Select is larger than N-Active? (10 points)

To minimize misalignment

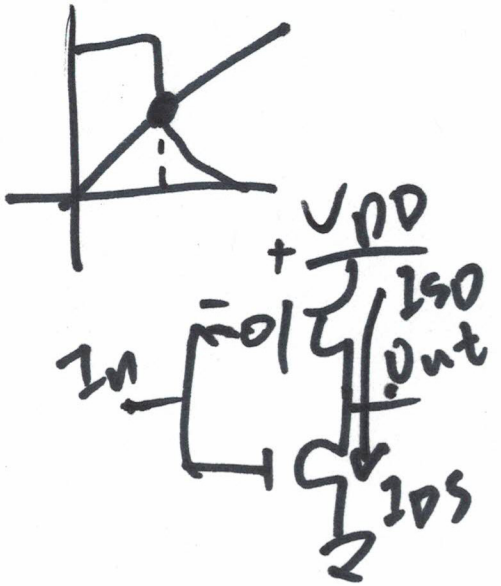
8. Can a polysilicon wire be used as resistors? How to reduce the resistance of a polysilicon wire? (10 points)

CS: Poly resistance 200Ω/square

Deposit siliciide on the top of poly



switching Point of Inverters



$$V_{in} = V_{out} = V_{sp}$$

$$\frac{\beta_p}{2}(V_{DD} - V_{sp} - V_{THP})^2 = \frac{\beta_n}{2}(V_{sp} - V_{THN})^2$$

$$V_{sp} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{THN} + (V_{DD} - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = 2{,}5V$$

$V_{sp} = 2.5V$

10 K range

$$\frac{3{,}3V}{5} = \frac{R_2}{R_1 + R_2}$$

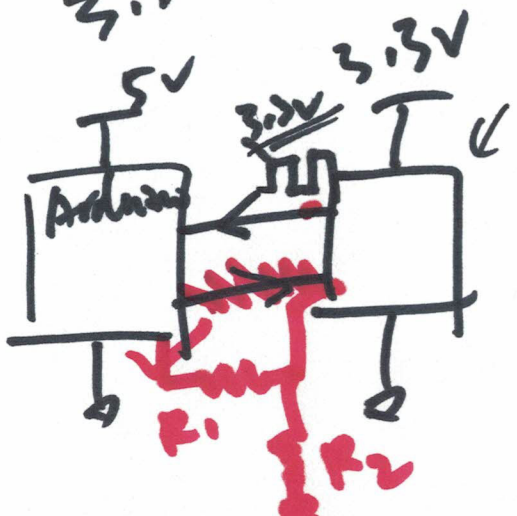
$$\sqrt{\frac{\beta_n}{\beta_p}} \approx 1$$

$$\frac{KP_n}{2}\frac{W_n}{L_n} = \frac{KP_p}{2}\frac{W_p}{L_p}$$

$$\begin{cases} KP_n = 120\,\mu A/V^2 \\ KP_p = 40\,mA/V^2 \end{cases}$$

5V Arduinos

3,3V.



Reduce the life-span