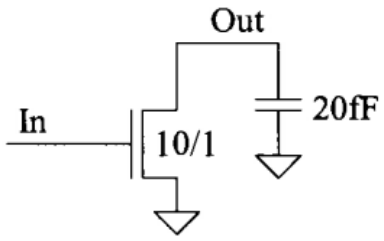
CE338 Homework 7

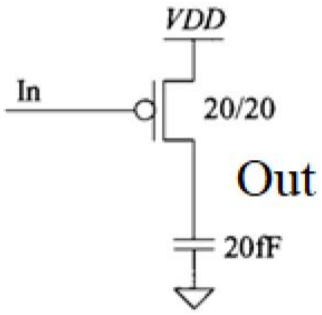
1. For the following circuits estimate the delay at the output. Use the 50 nm (short-channel CMOS) process. (Table 10.2 is from the CMOS text book on page 320). Assume that the capacitor in (a) stores a VDD as the initial value before the NMOS turns on and the capacitor in (b) stores 0 as the initial value before the PMOS turns on. (40 points)

Table 10.2 Parameters for general digital design using the long-channel (scale factor is 1 μm) or short-channel (scale factor of 50 nm) CMOS process **used in this book**.

Technology	Drawn	Actual size	$R_{n,p}$	$C_{ox,n,p}$
NMOS (long-channel)	10/1	10 μm by 1 μm	1.5k	17.5 *fF*
PMOS (long-channel)	30/1	30 μm by 1 μm	1.5k	52.5 *fF*
NMOS (short-channel)	10/1	0.5 μm by 50 nm	3.4k	625 *aF*
PMOS (short-channel)	20/1	1 μm by 50 nm	3.4k	1.25 *fF*



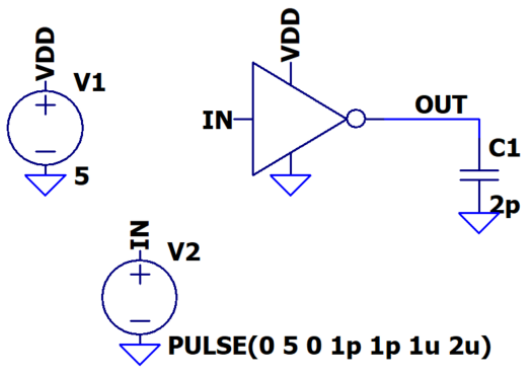
(a)



(b)

2. Draw the resistive/capacitive digital model of **ONE pair** of inverters and estimate the oscillation frequency of a 7-stage ring oscillator. NMOS: Rn = 3.4 k, Coxn = 0.625 fF. PMOS: Rp = 3.4 k, Coxp = 1.25 fF. (30 points)

3. What is the dynamic power dissipation of the following circuit? (Assume the inverter has adequate current to drive the load capacitor, also Cload = Ctot) (30 points)


VDD
V1
5
VDD
IN
OUT
C1
2p
IN
V2
PULSE(0 5 0 1p 1p 1u 2u)