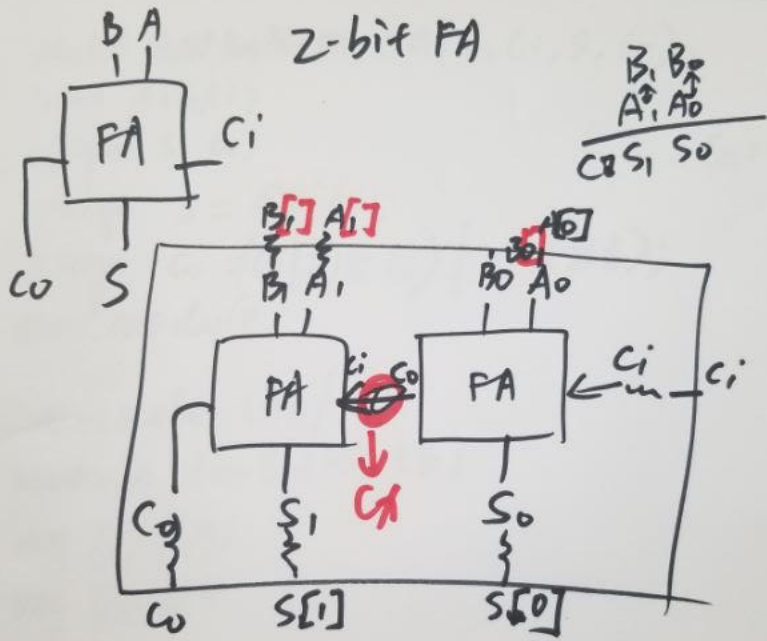


2-bit FA



```
Module Gate OneBitFA (A, B, Ci, S, Co);  
input A, B, Ci;  
output S, Co;  
assign S = A ^ B ^ Ci;  
assign Co = (A | B) & Ci | (A & B);  
end module
```

$$Co = (A + B) Ci + AB$$

```
`timescale 1ns/1ps  
module twoBitFA_tb;  
reg [1:0] A;  
reg [1:0] B;  
reg Ci;  
wire [1:0] S;  
wire Co;  
wire Cx;
```

(2)

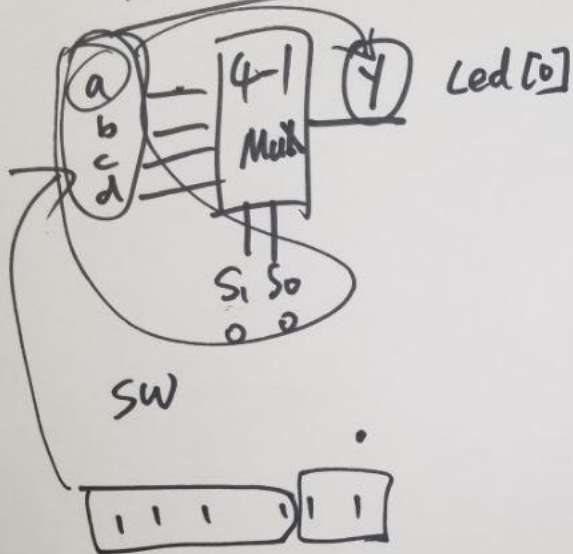
initial begin $B[i:0] = 2'b0; A[i:0] = 2'b0; C_i = 0;$
for ($i = 0; i < 32; i = i + 1$)
begin

~~$B[i], A[i], C_i$~~
 $\{ B_{[i:0]}, A_{[i:0]}, C_i \} = \{ B_{[i:0]}, A_{[i:0]}, C_i \} + 1;$

end

end

4-1 MUX



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