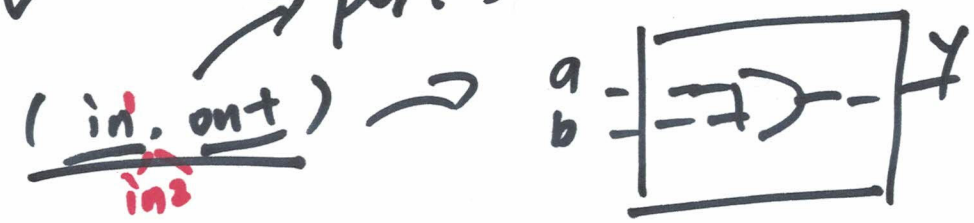
Verilog : .v

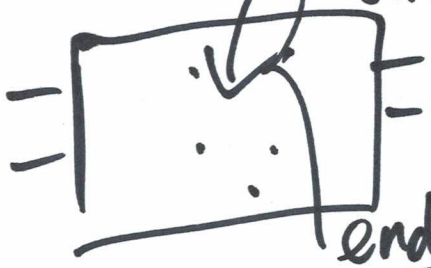
Name of the module

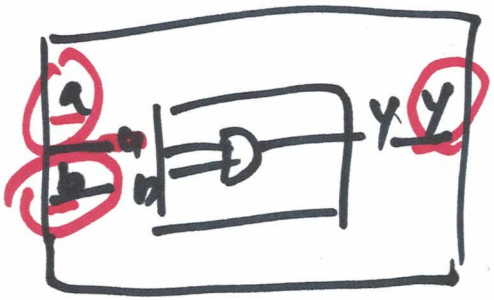
```
module andGate ( in1, in2, out )
input in1, in2;
output out;
assign out = in1 & in2;
endmodule
```

ports



&





o

testbench .v

in1/in2

`timescale

```
module andGate_tb;
reg a, b;
wire Y;
andGate UUT ( .a(a), .b(b), .Y(Y) )
initial begin
#5; a=1'b0; b=1'b0;
#5; a=1'b0; b=1'b1;
#5; a=1'b1; b=1'b0;
#5; a=1'b1; b=1'b1;
end
endmodule
```

test.v

```
module andGate
endmodule
module orGate
endmodule
:
:
:
```

andGate.v

```
module andGate
```

end module

orGate.v

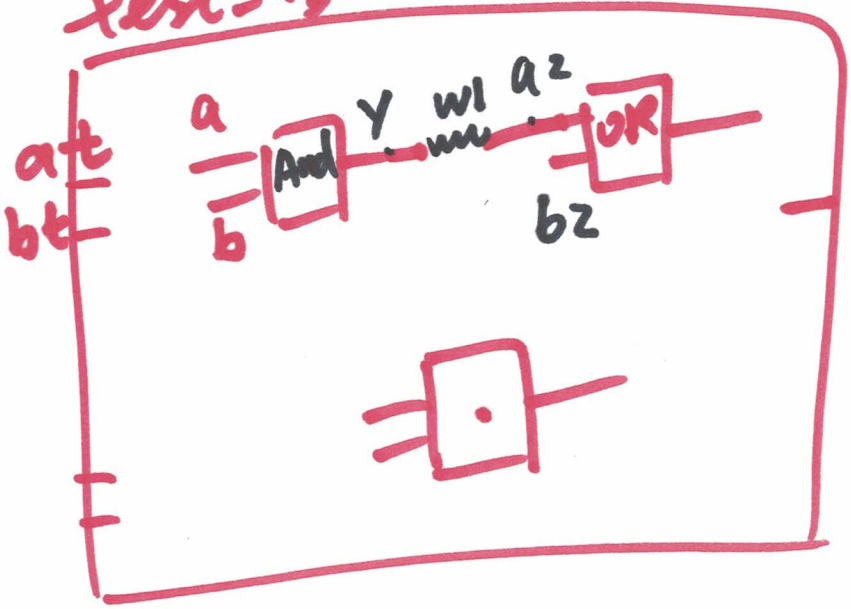
```
module orGate
```

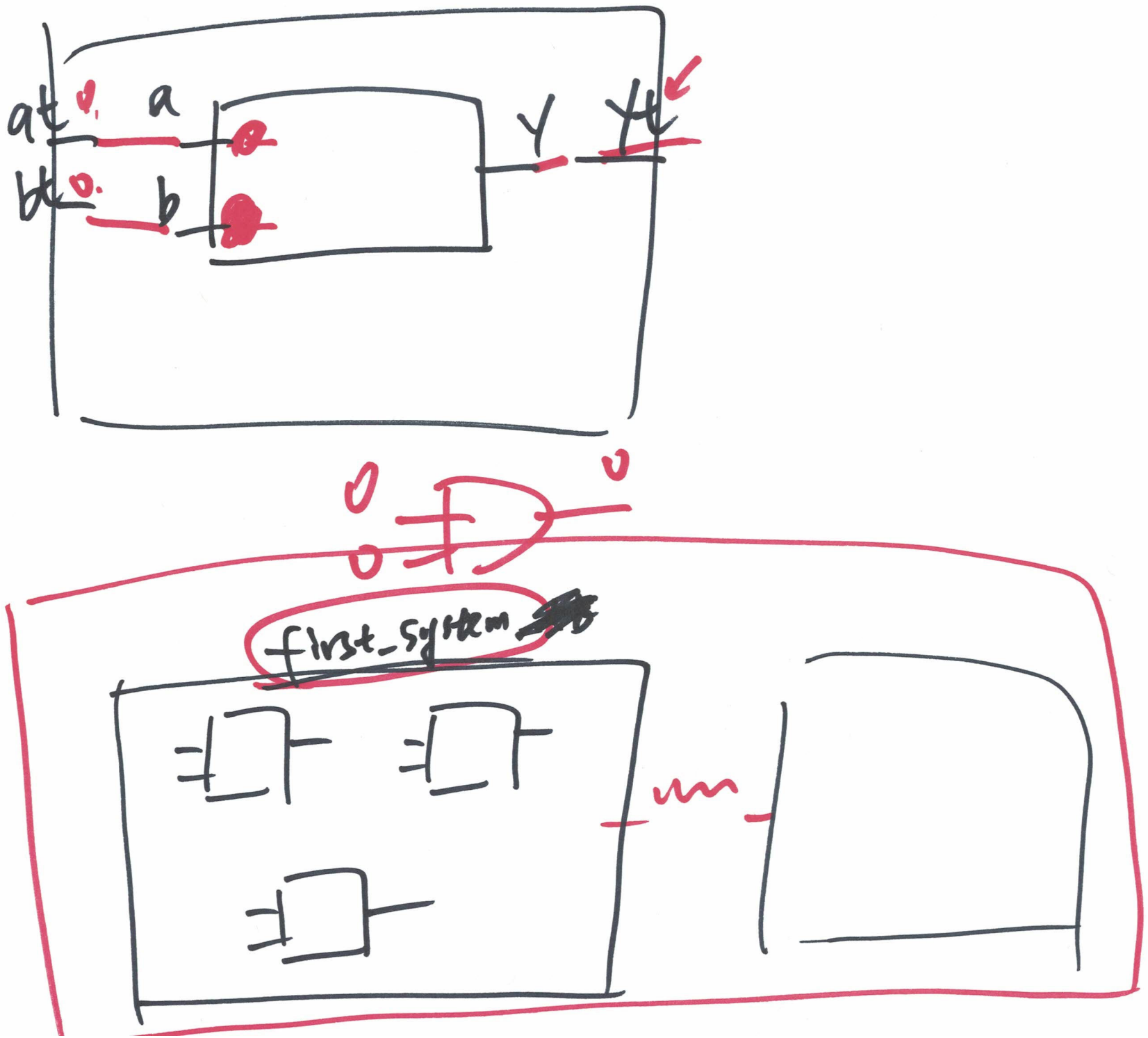
endmodule

test_tb.v

```
reg at, bt;
wire w1;
andGate UUT1 (.Y(w1), .a(at), .b(bt),
orGate UUT2 (.a2(w1),
xorGate UUT3 (
```

test_tb.v




a
b
Y
first_system